

RISC-V Instruction Set Architecture becoming Ubiquitous in Space Processors

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General Manager



A world leader in embedded computer systems for harsh environments



Experts in fault-tolerant computing



We provide a full ecosystem to support hardware and software development



Implementing SPARC and RISC-V architectures





Established 2001 as a spin-off from
Chalmers and European Space Agency



Located in Gothenburg, Sweden



75+ employees in Sweden, Germany,
France, Spain, and United Kingdom



In-house facilities

- Hardware design
- Software design
- Component laboratory

Why processors in space?

A detailed image of a Mars rover, likely a Curiosity rover, on the surface of Mars. The rover is a six-wheeled vehicle with a complex mechanical structure, including a mast with various sensors and cameras. It is positioned on a rocky, reddish-brown terrain under a hazy, orange sky. The rover's shadow is cast on the ground to its right.

They enable everything on our space missions!

A person wearing a white lab coat and blue nitrile gloves is holding a square microchip. The chip has a grid of gold pins on its underside and a central square area with intricate circuitry. The background is a soft-focus laboratory setting with various pieces of equipment.

What is the semiconductor crisis?

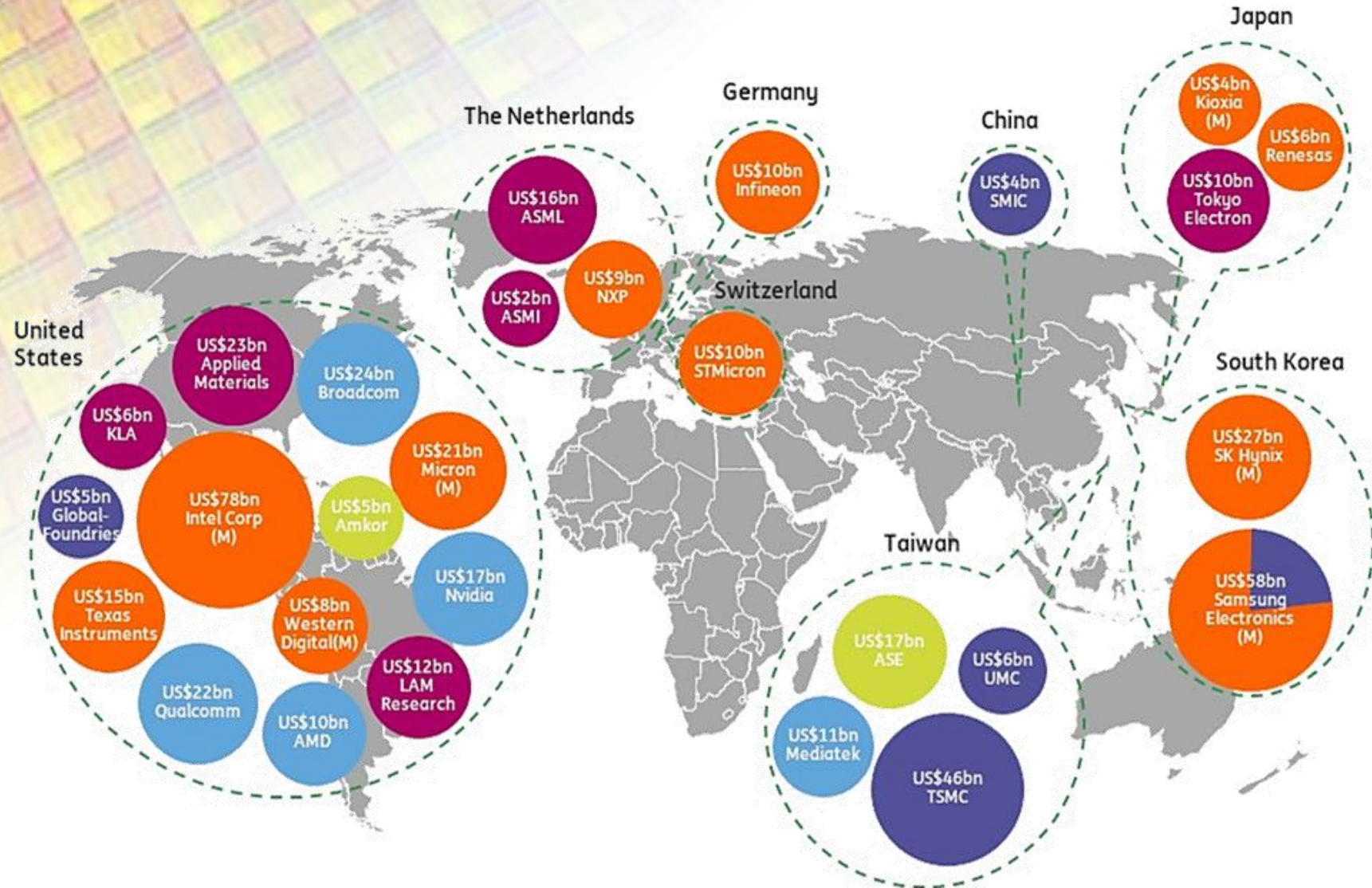
Disruptive technology gets a whole new meaning.

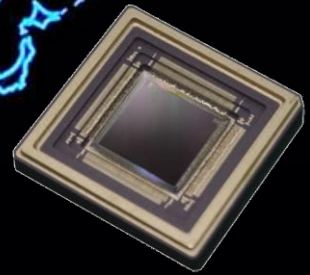
The geopolitical map of semiconductors

Less globalization, more localization



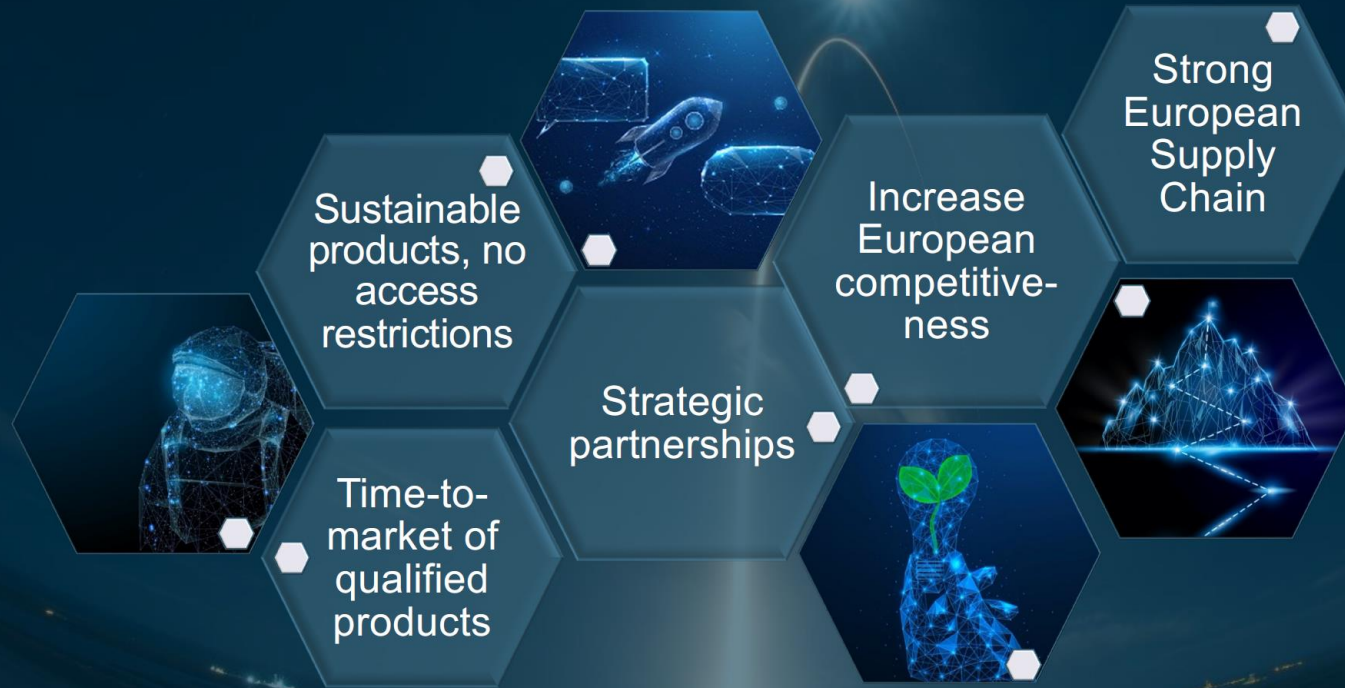
**THE EU CHIPS ACT &
TECHNOLOGICAL
SOVEREIGNTY**





Each region is now developing space processors

European Sovereignty Initiative



→ THE EUROPEAN SPACE AGENCY



EEE Space Component Sovereignty for Europe
Electrical, Electronic and Electro-mechanical (EEE)

What is RISC-V® and why is it important?

An Instruction Set Architecture (ISA) specifies what the processor must do in response to an instruction from the software.

“ISA is where software meets hardware”

RISC-V is an open ISA that is freely available to industry, just like SPARC that is used on most spacecraft.

RISC-V is the fifth edition architecture from UC Berkeley.

Why is RISC-V® winning?

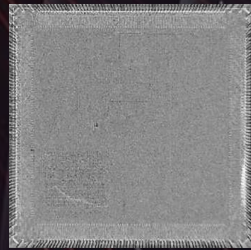
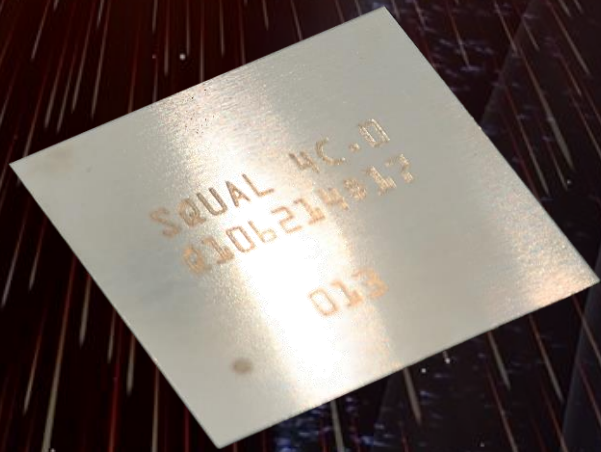
Key winning features

- Open
- License-free and royalty-free
- Adaptable with custom extensions (instructions)
- Less complex – flexible and adaptable

The flexibility and open nature of RISC-V has allowed it to be adopted fast into the electronics industry, for example Nvidia to ship a billion of cores in 2024. A promising future for space usage!

Where are we with RISC-V® in Space?

Radiation hardened RISC-V test chips already exist in Europe!
RISC-V technology is already flying on European missions!

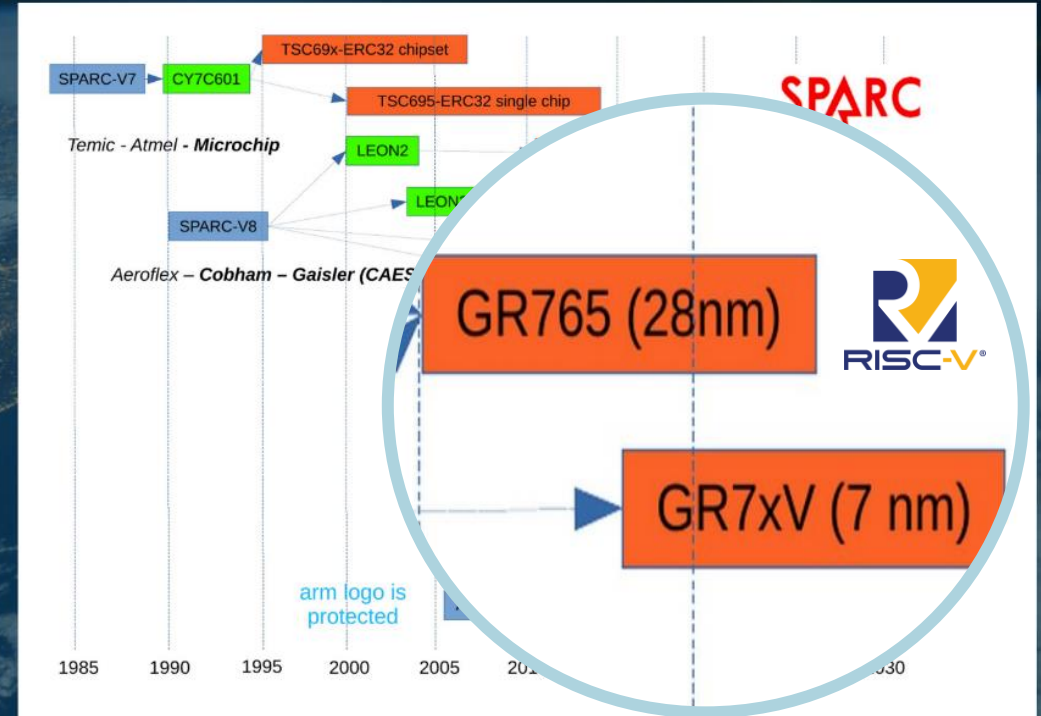


2021/22: RISC-V@ESA in Fast Forward Mode

- Concept study for GR7xV HPC started in ARTES in 2021
- Target 7 nm – technology not available for space
- 2022 started with a “shoestring” ITT in TDE: 450k€
- Can we do RISC-V prototypes in 22-28 nm technology?
- Synergy with GR765 (originally planned as 8-core LEON5 only)
- → RISC-V is **hitch-hiking** on SPARC, saving cost...
- Only CPU cores are duplicated, but cache RAM and SoC share
- **Facilitates transition for users: one chip, one board, two modes**
- GR765 phase 2 released with ARTES funding also in 2022
- Today ~ 4 M€ public funding committed into GR765 / GR7xV
- complemented by significant co-funding
- Prototypes funded, flight parts (ROM cost 4.5 M€) TBC

Space Micropocessor Roadmaps in Europe

- Almost 30 years of SPARC
- LEON chips by Microchip and Cobham Gaisler (CG)
- CG transition to RISC-V
- RISC-V on Microchip PolarFire-SoC FPGA
- NASA HPSC-new opted RISC-V (SiFive/Microchip)
- NX roadmap: ARM
- ARM also on Xilinx FPGA



Ultra Deep Sub-Micron

Ultra Deep Sub-Micron roadmap
ASIC, FPGA, and RISC-V Microprocessors

Space complex EEE – Chiplet approach

- High level of integration, high costs of fabrication re packaging solutions that would represent an alternative integration
- For the development of the FPGAs, microprocessors is represented by the chiplet approach:
 - High levels of integration
 - Flexibility to re-use key IPs for other future products
 - Flexibility to optimize specific functions, IPs, as a function speed, power consumption,...)
 - Cost savings on the long term
- COM-DEFIS will initiate developments for the next Microprocessors based on chiplet architecture

EU Strategy for Space Processors



- Currently, Commercial-of-the-Shelf (COTS) processors viable in LEO application offer significant cost advantage, however they require screening, dedicated radiation mitigation and error handling
 - Mostly non-EU solutions
 - Not suitable for security sensitive and Institutional space missions
- European Commission objective to develop EU based mixed-signal standard cells library and IPs portfolio relevant for FPGA, ASICs based on 7nm technology
 - Increase and secure competitiveness of EU space industry in Telecom, Nav and EO payloads in response to EU space missions
 - Cover the full spectrum of orbits LEO, MEO and GEO for insertion of EU institutional space missions



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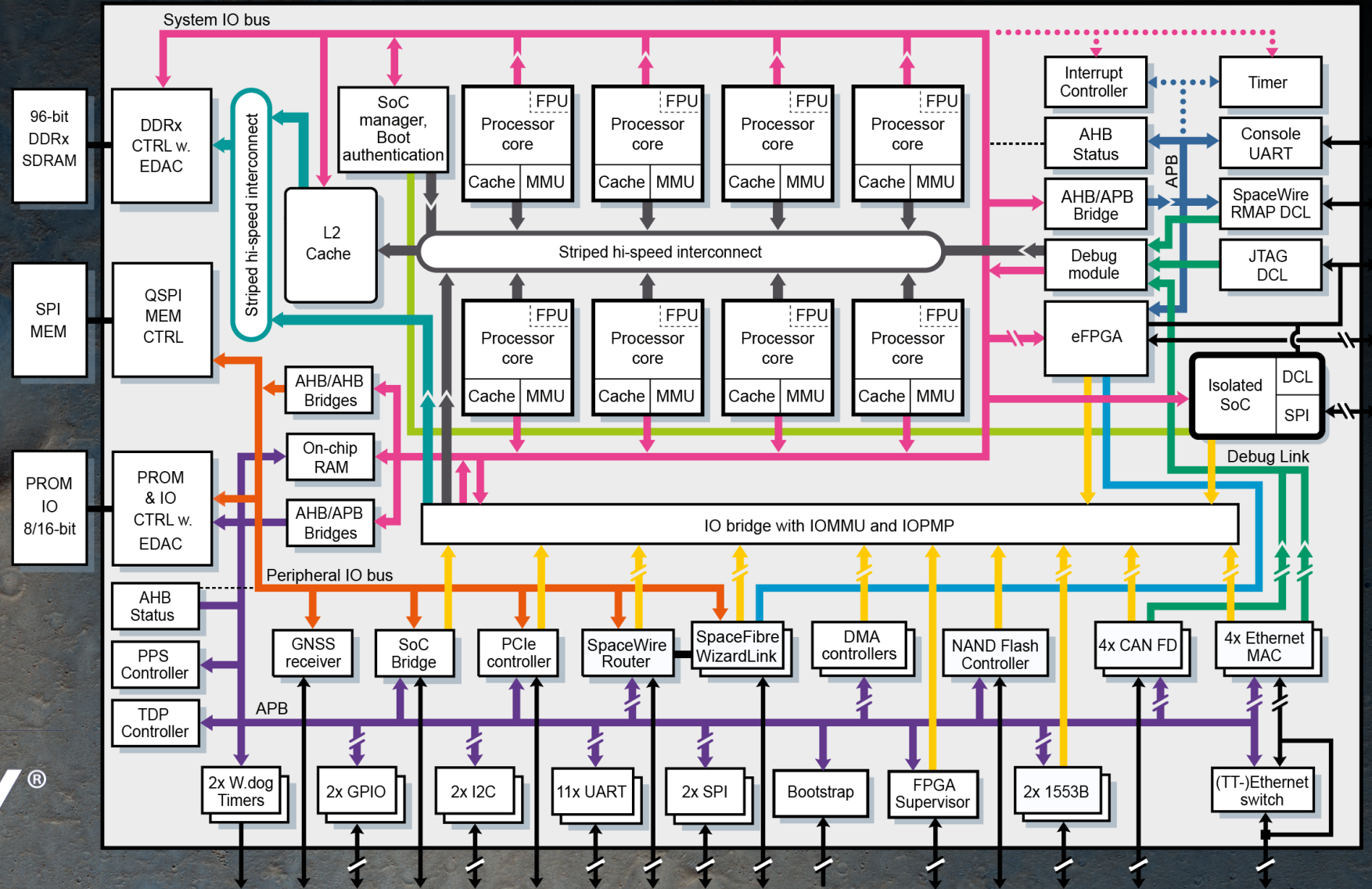
Space Complex EEE - Chiplet 7 nm

EU Strategy for Space Processors

GR765 – European 8-core space processor available in 2025!



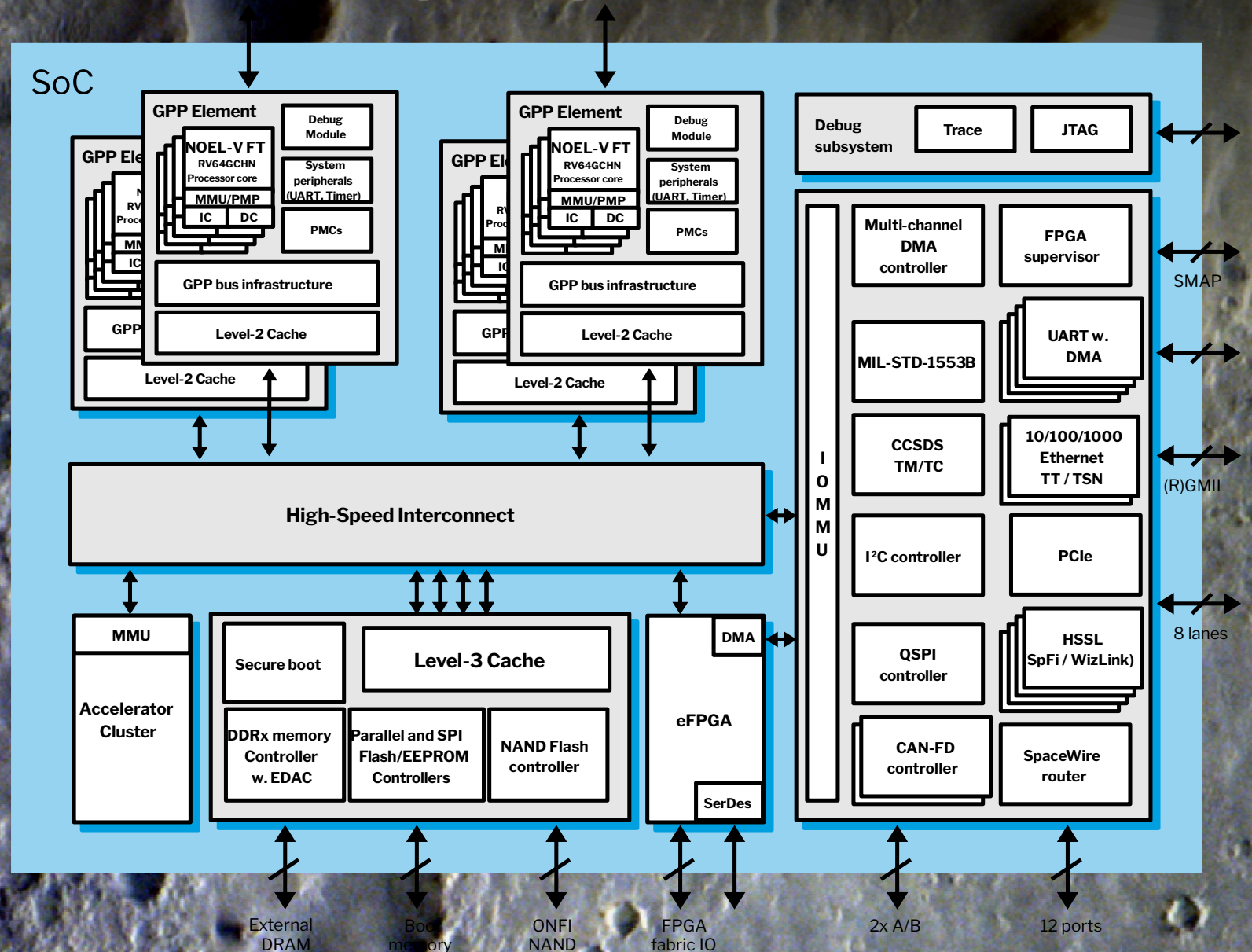
SPARC
RISC-V®

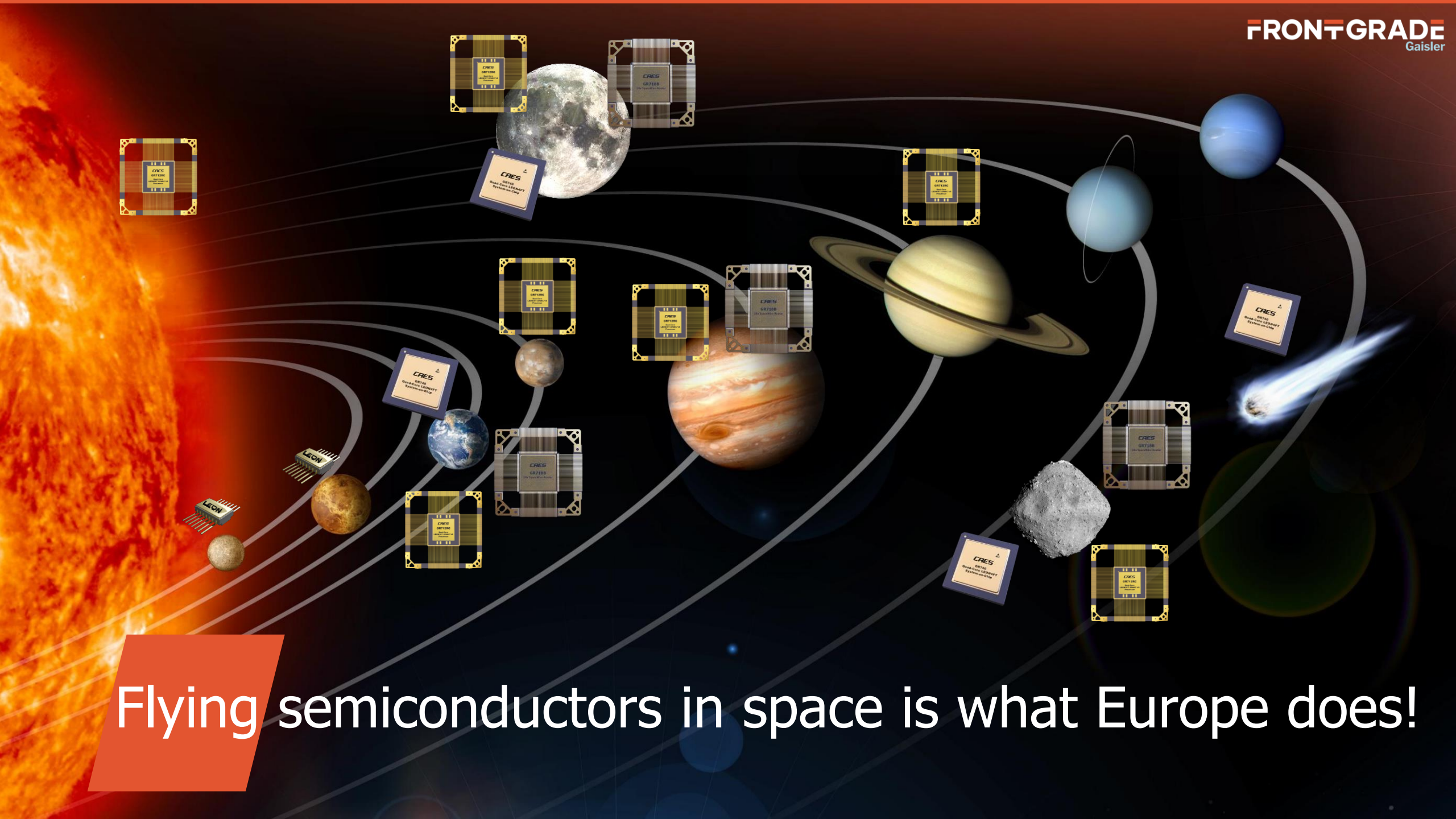


GR7xV – Next generation 16-core space processor on 7nm!



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Flying semiconductors in space is what Europe does!

The second **RISC-V in Space Workshop**
will take place in Gothenburg, Sweden,
on 2-3 April 2025.



Workshop April 2-3, 2025 | Gothenburg



Thank you for your attention!