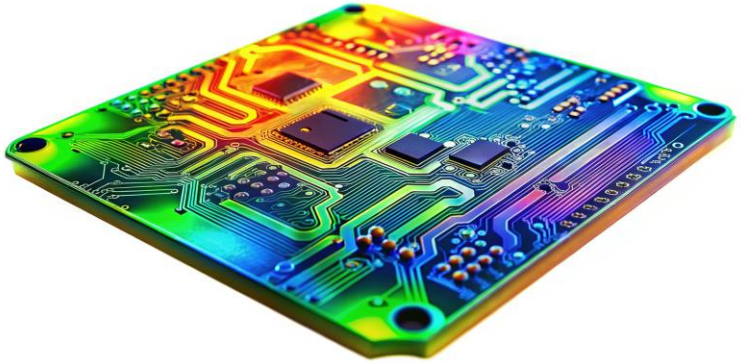
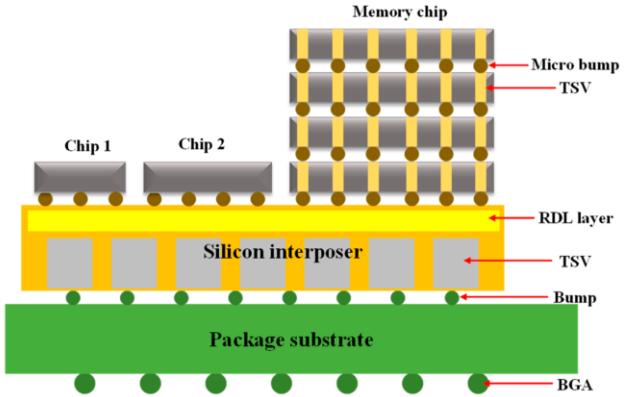
Measurement and Metrology challenges in 3D Heterogeneous Integrated Circuits

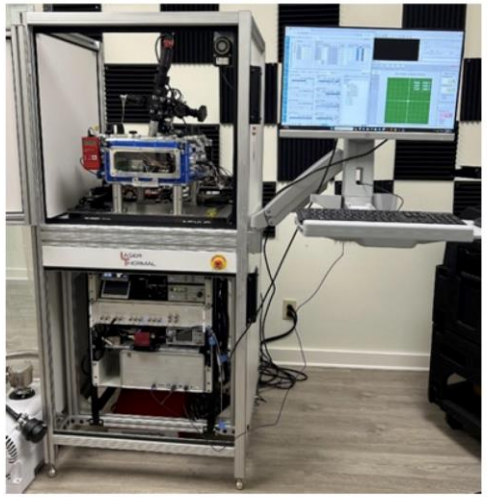
John Gaskins, CEO and co-founder, Laser Thermal

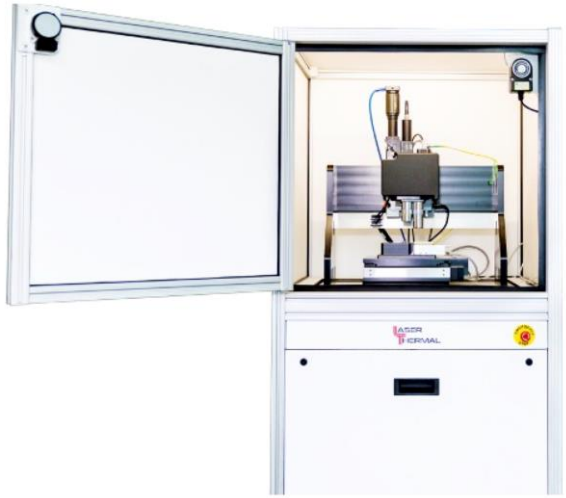




https://doi.org/10.3390/mi14061149

Thermal Characterization from the Package to Transistor Level





Nanometer

NTM

FASTR

TOPS

Bulk

Nano-probe Thermoreflectance Microscopy (NTM)

Available Q4 2026

Sub-50nm resolution, bonded interfaces, active devices, temp and thermal properties

Frequency And Steady-state ThermoReflectance (FASTR)

Commercially Available

Thin-film to bulk thermal properties, thermal property mapping

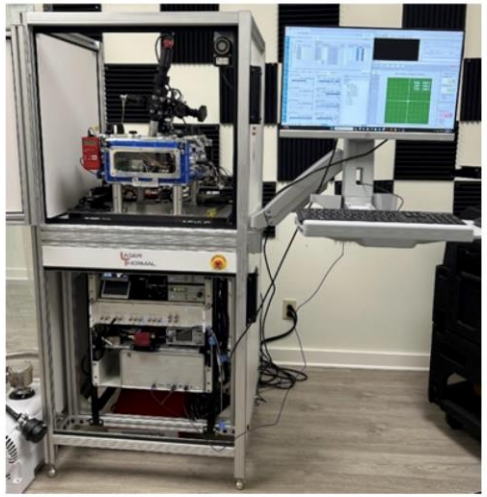
Thermo-Optical Plane Source (TOPS)

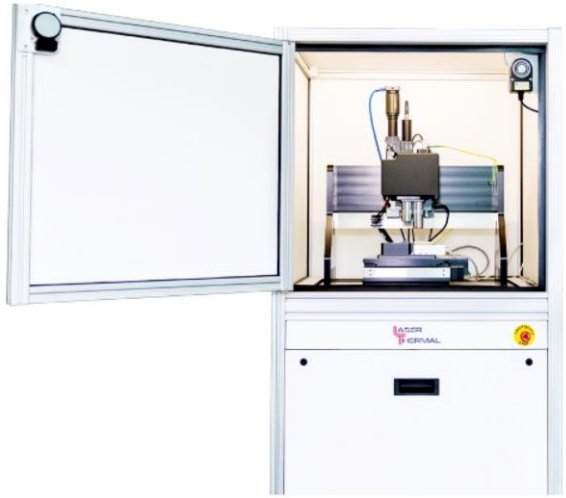
Commercially Available

TIMs, liquids, pastes, bulk material, packaging applications

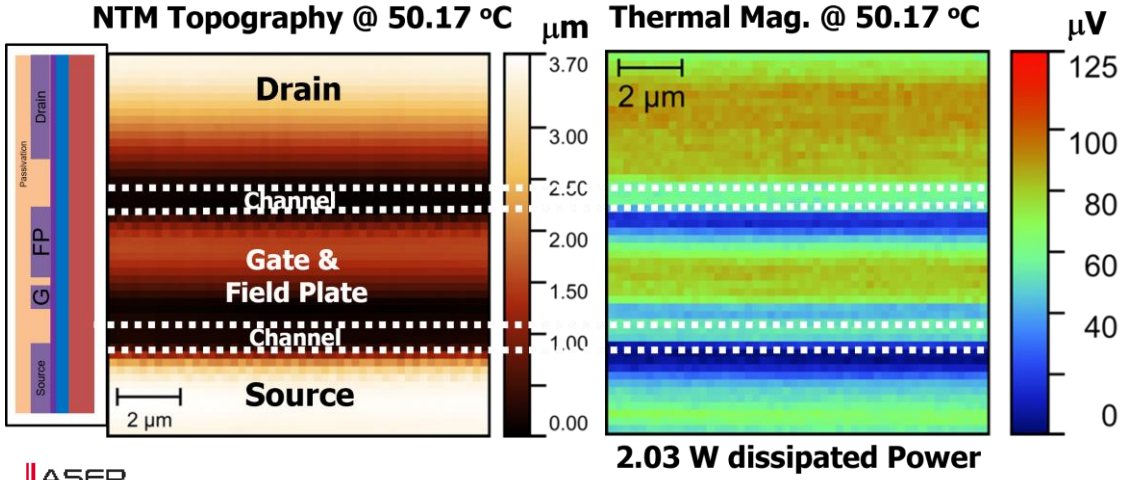
LASER THERMAL

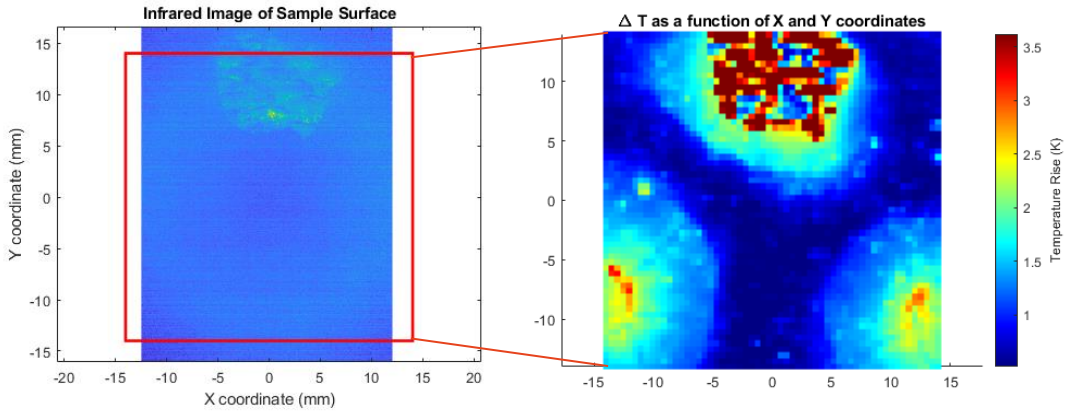
Thermal Characterization from the Package to Transistor Level



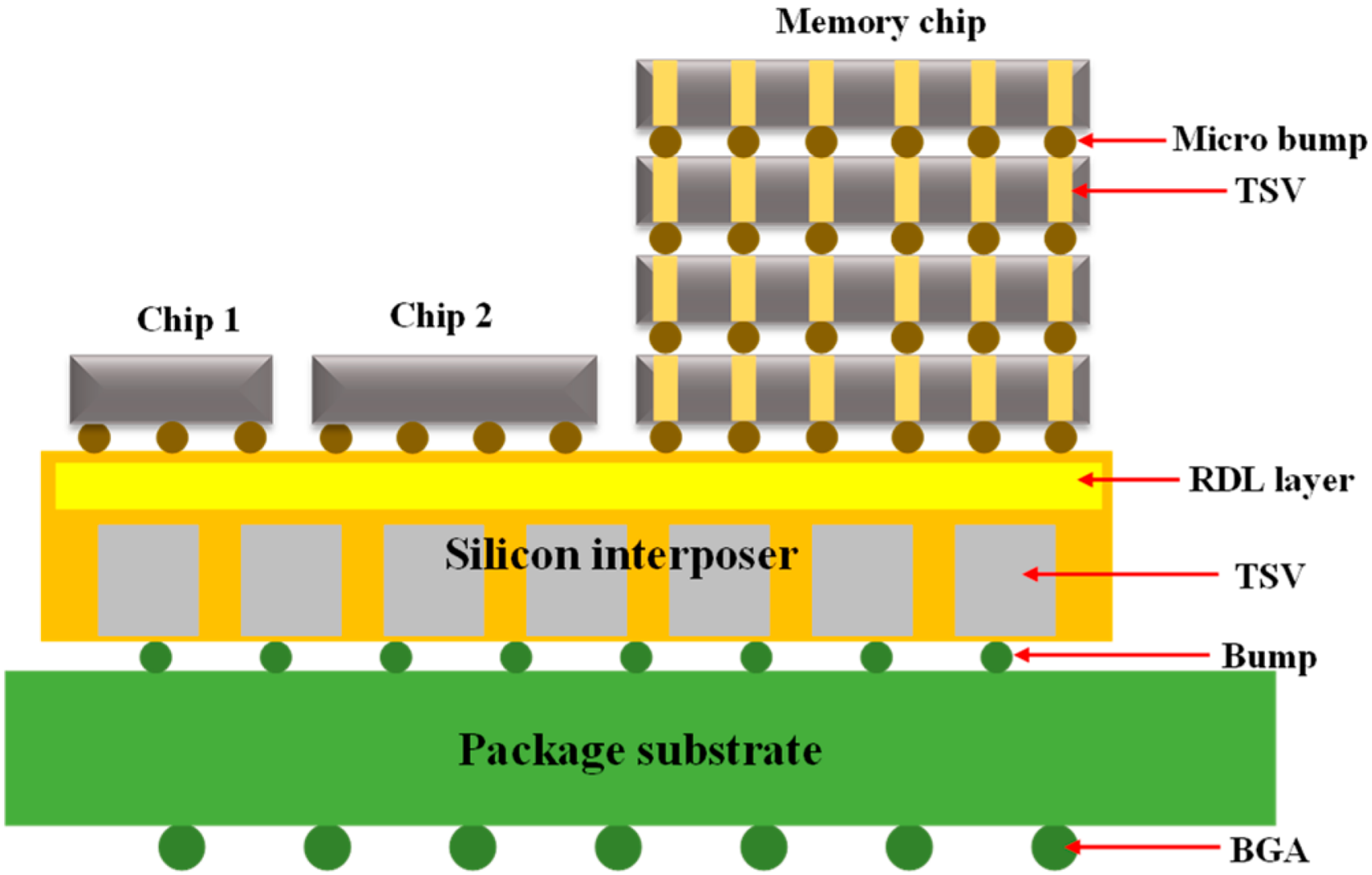


Nanometer — NTM — FASTR — TOPS — Bulk





What is a 3D Heterogeneous Integrated Circuit (3D HIC)?



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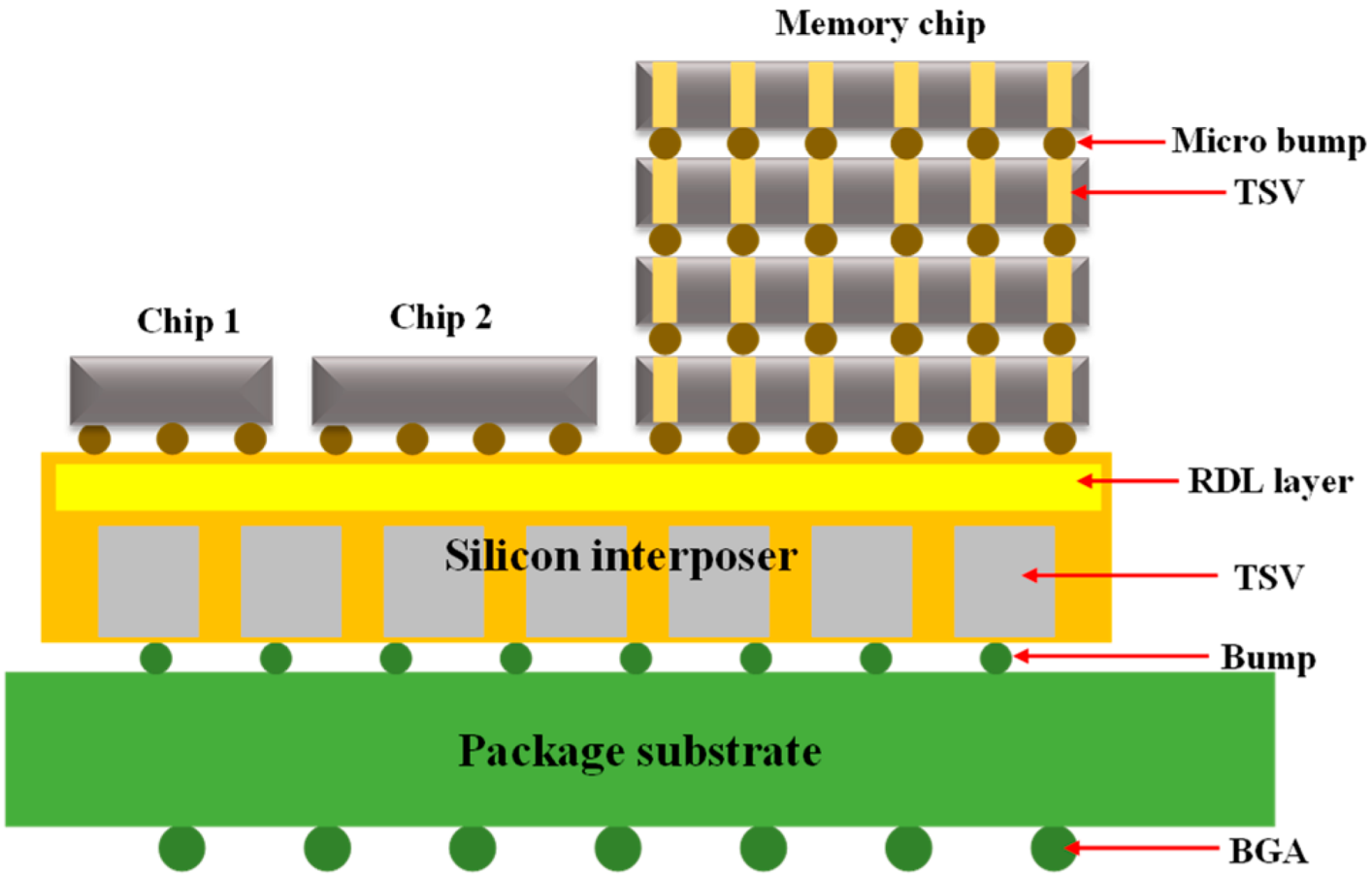
Challenges introduced by 3D HIC



- High-Power Densities
- Restricted Heat Dissipation Pathways
- Thermal Crosstalk
- More Interfaces = More Resistance
- Integration Challenges with Advanced Cooling Solutions – Air Cooling insufficient
- Thermal Cycling Reliability Issues

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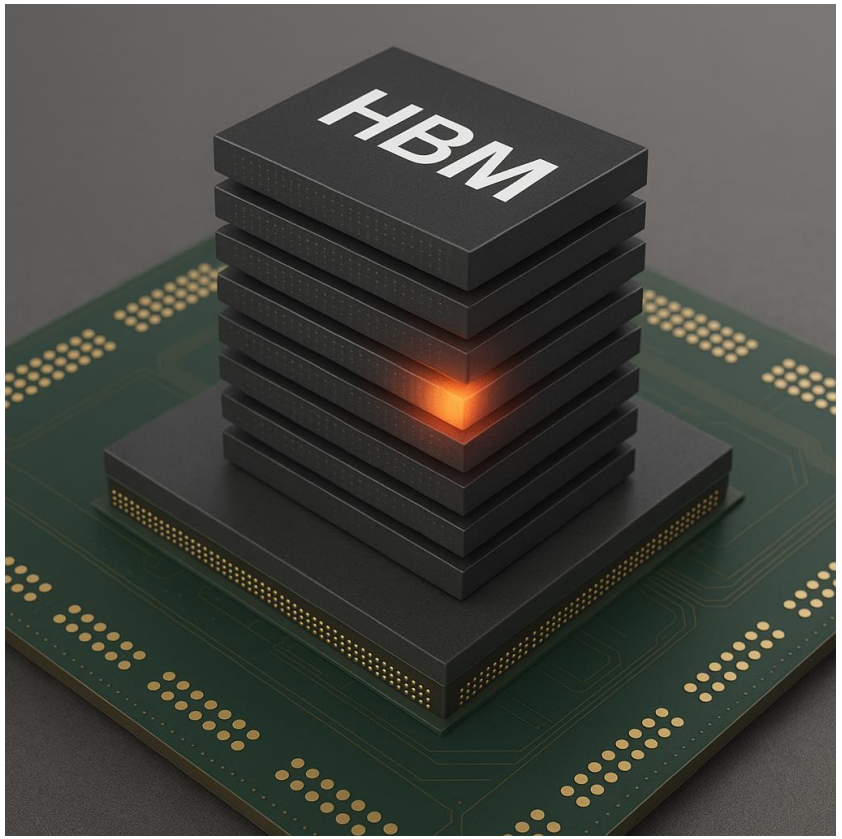
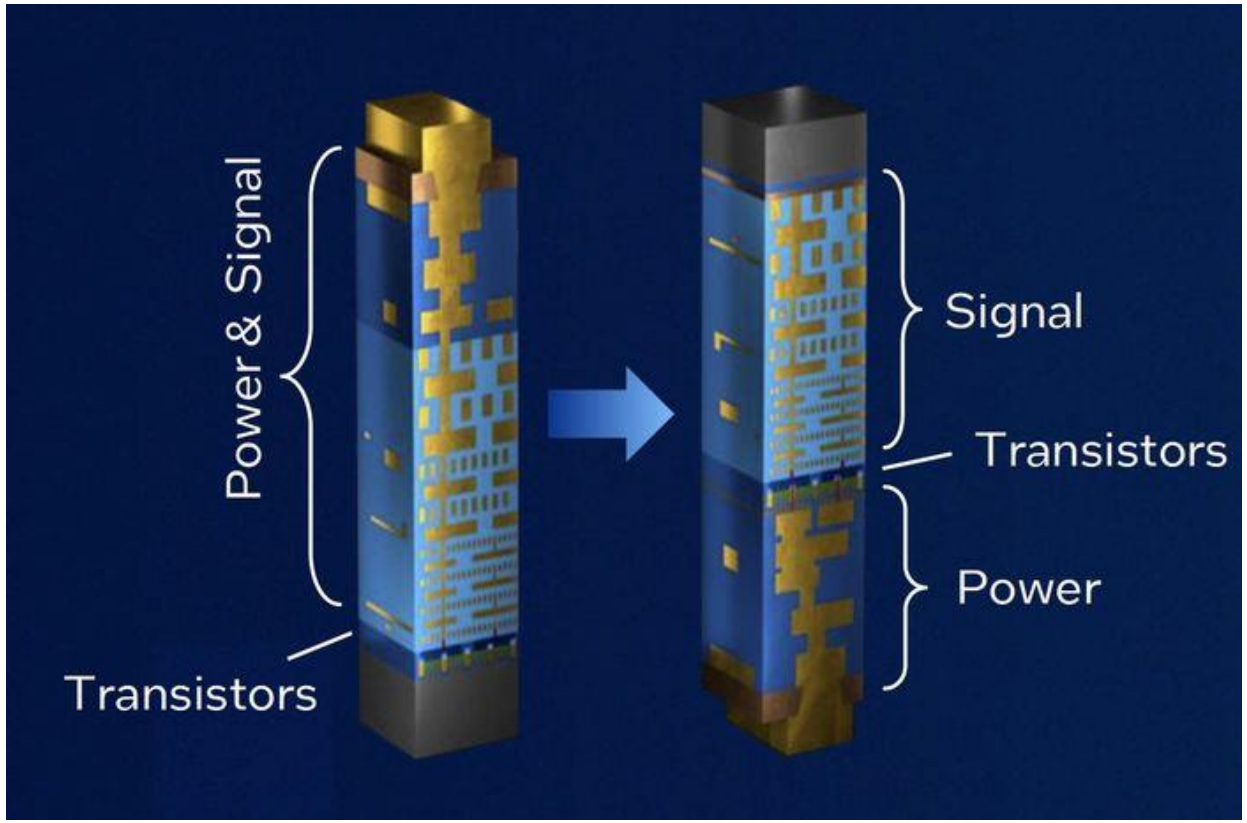
Existing Metrology Issues in HBM/3D HIC

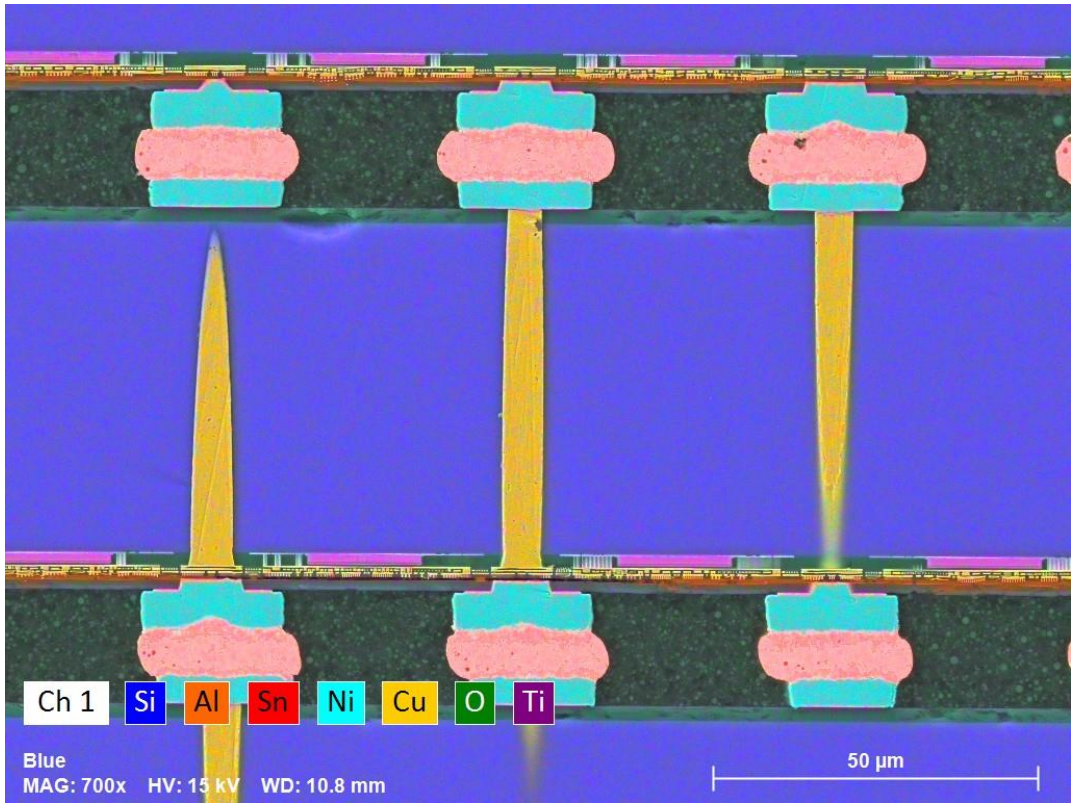


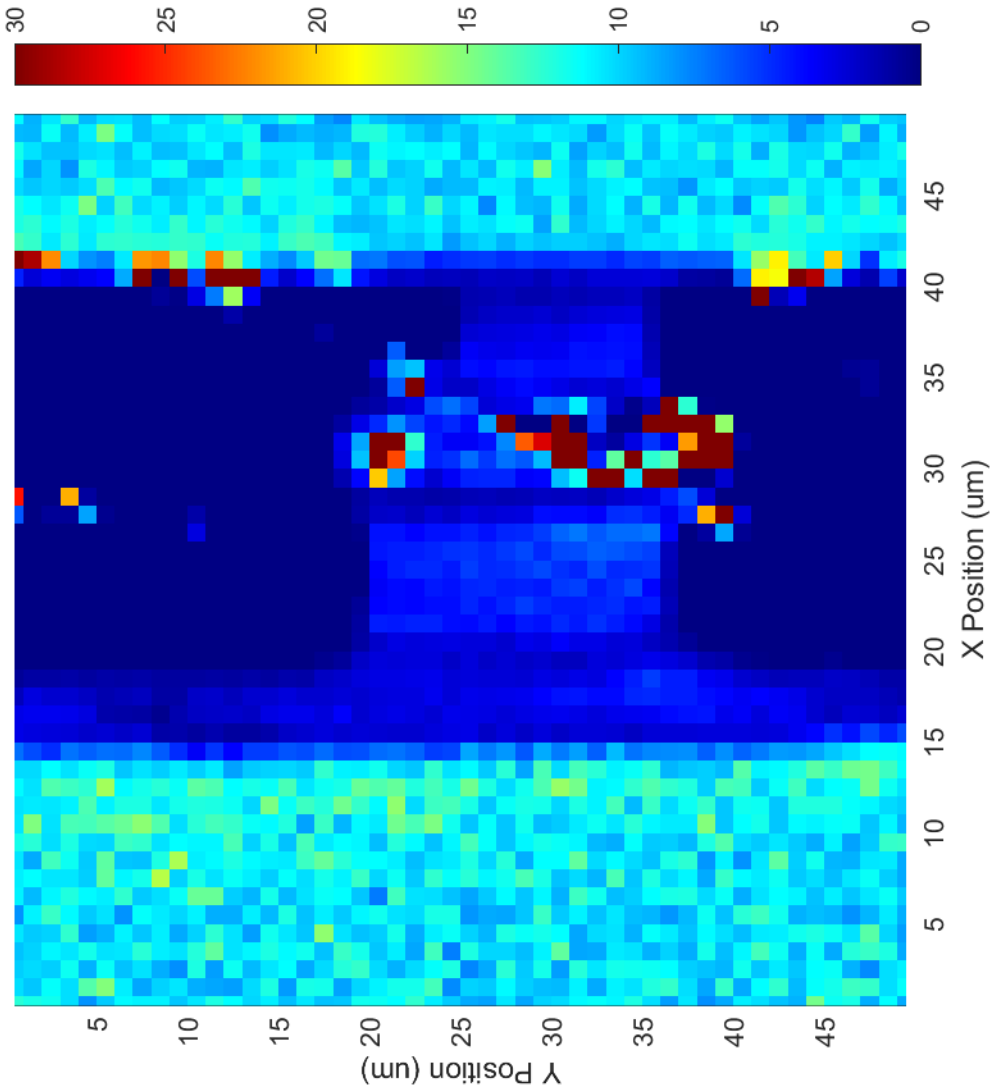


How do we “see” sub-surface defects and hot-spots?

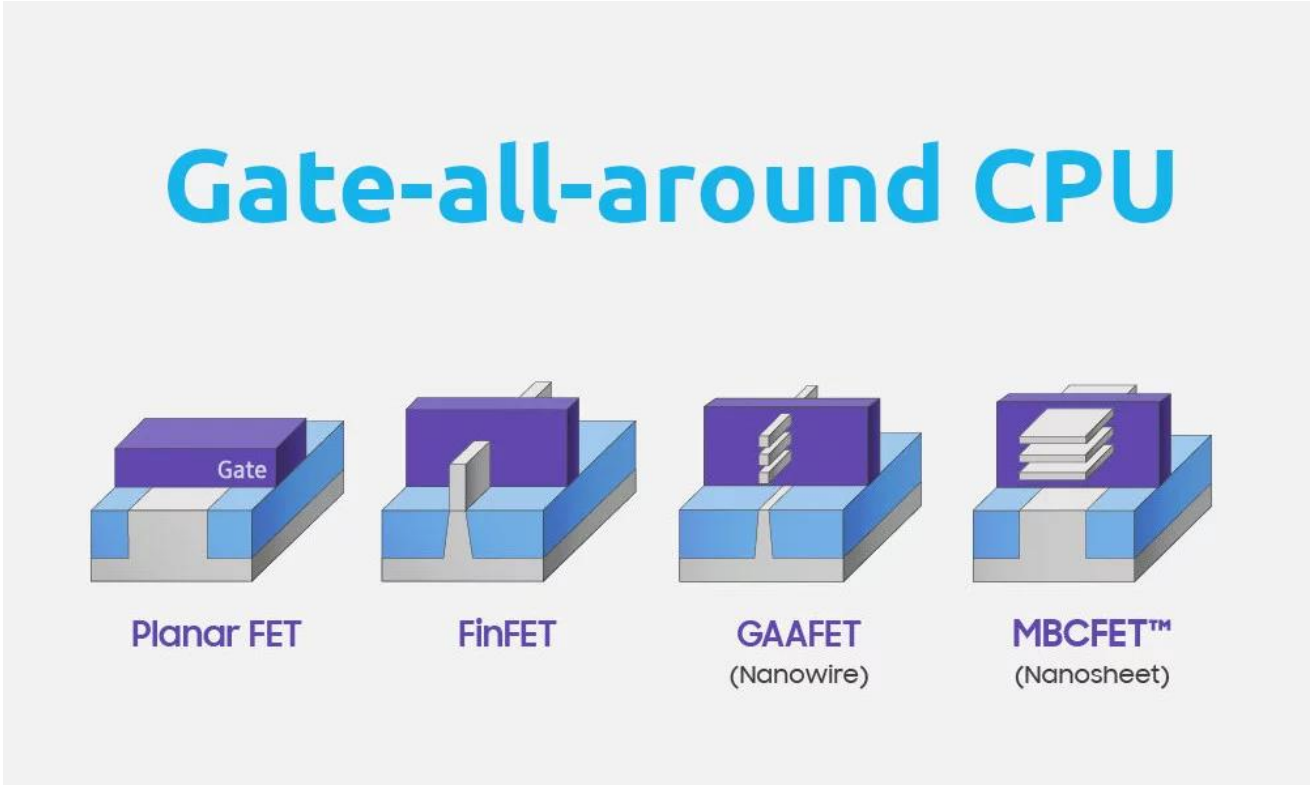
How do we assess the quality of next gen bonding and joining techniques?

Understanding properties as they are integrated





Existing Characterization Issues in 3D HIC



Thermal standards do not exist at almost any scale, let alone small scales!

New materials for new device architectures must be measured!

https://techplanet.today/post/what-is-gate-all-around-cpu

Come visit us to discuss your thermal measurement challenges

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