WD Advanced Materials

Material Solutions for Microelectronics

DIAMOND

Quantum | Thermal | Ultra-Wide Bandgap Semiconductor

JOHN CIRALDO | CHIEF TECHNOLOGY OFFICER

Ceramics Expo | Thermal Management Expo
April 30, 2025

WDAM's Growth Journey

LAYING THE FOUNDATION | ENHANCING INFRASTRUCTURE | ACCELERATING GROWTH

2009 — WD is founded, leveraging CVD technology a decade in the works

2011 — Team expands to include new executive leadership

2013 — Continued R&D refines production processes and improves yields

2015 — 9-carat CVD diamond breaks world records

2017 — Production expands in gemstone and Advanced Materials

2019 — WD is the first to be certified by SCS-007

Certified SUSTAINABILITY RATED DIAMONDS

2021 — DARPA LADDIS program awarded, grant work accelerates

2023 — WD relaunches as WD Advanced Materials LLC

Formalized worldwide exclusive patent license agreement with the Carnegie Institution for Science in Washington

CARNEGIE SCIENCE

WD sells its first gemstone-quality lab grown diamond

Capacity expands 3x through high-ROI chamber build

Huron Capital investment provides capital to drive growth

WD acquires J2 Materials, driving scale and expansion of WD's Advanced Materials division

AM Advanced Materials WD LAB GROWN DIAMONDS

International growth accelerates via our Distributor and Advanced Materials networks

Established Infrastructure and Operations

STATE-OF-THE-ART FACILITY

- Centralized control room and monitoring stations
- Dedicated diamond chambers and laser rooms

Automated Operations

PROPRIETARY GROWTH CHAMBERS

- 100s of CVD chambers designed and built in-house
- Dedicated post-processing 65+ unit laser room, with raman, optical microscopy, polishing and XRD

Laser Room

CONSISTENT QUALITY AT SCALE

- Automated systems, software and trained staff ensure consistency at ~20K+ wafers/month
- Streamlined quality assurances processes

Quality Control Center

MULTIPLE FACILITY REDUNDANCIES

- Redundancy ensures uninterrupted power distribution for all production equipment

Generators

EXPERT STAFF

- Academic and Operational experience drives technology and R&D leadership
- Over 100 years of combined diamond growing experience supporting our 15+ year operations
- Renowned material science experts and engineers specializing in CVD diamond growth

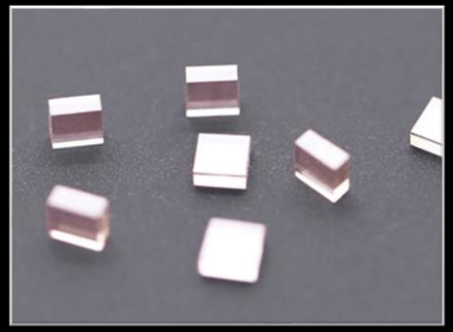
ENVIRONMENTALLY-FRIENDLY PRODUCTION

- Custom-built cooling system limits H20 consumption and maximizes chamber chilling efficiency

Chiller Unit

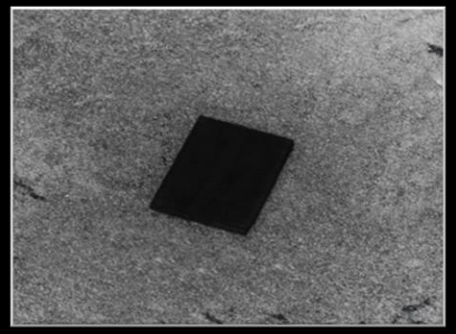
WDAM Single Crystal & Polycrystalline Diamond Products

High-quality diamond substrates, available to precise order specifications, at sizes ranging up to 25mm and beyond



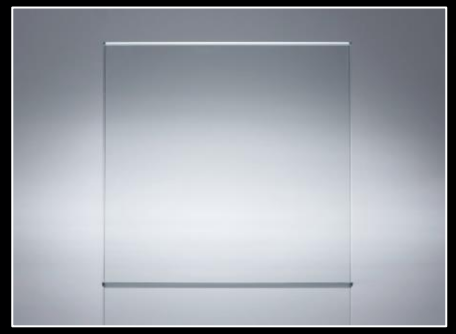
01_Quantum SCD

Isotopically pure film and bulk material featuring nitrogen vacancy (NV) centers, for use in next-generation technologies



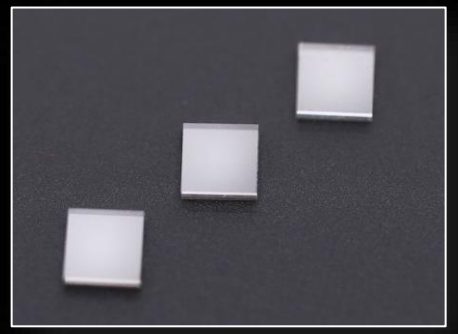
02_Conductive SCD

P-type boron-doped diamond wafers used across nano-indenters, deep-UV LEDs, and varied semiconductor devices



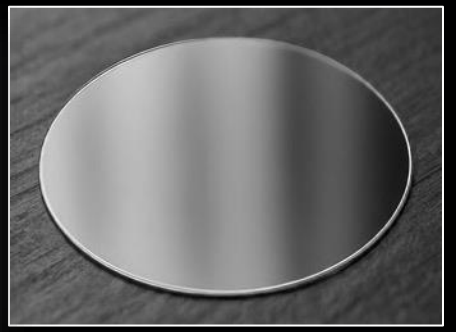
03_Intrinsic SCD

Ultra-pure, undoped electronic grade single crystal diamond substrates for use in sensitive thermal and optical applications



04_Optical SCD

Low-defect, low nitrogen diamond wafers for various scientific uses, including high-power electronics and surgical blades

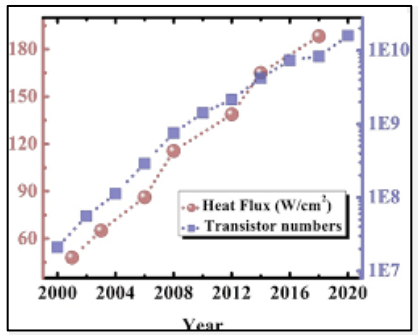


05_Polycrystalline

Thermal grade CVD polycrystalline diamond, available in film and bulk form, custom processed for advanced thermal applications

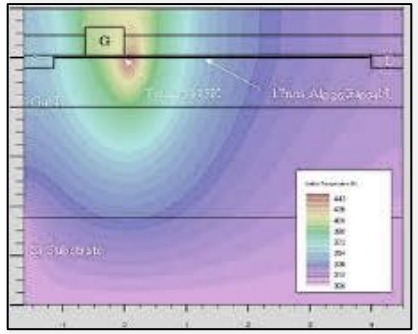
WD Advanced Materials

Chips Are Hot & They're Getting Hotter



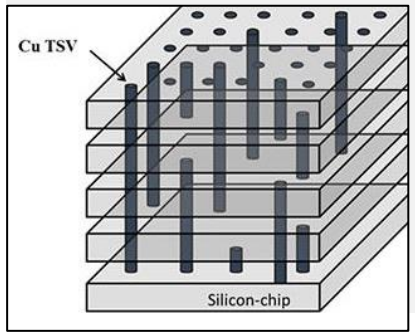
2D Chips

- Historical chip architecture
- Adherent to Moore's Law
  - As transistor count goes up, so does heat flux



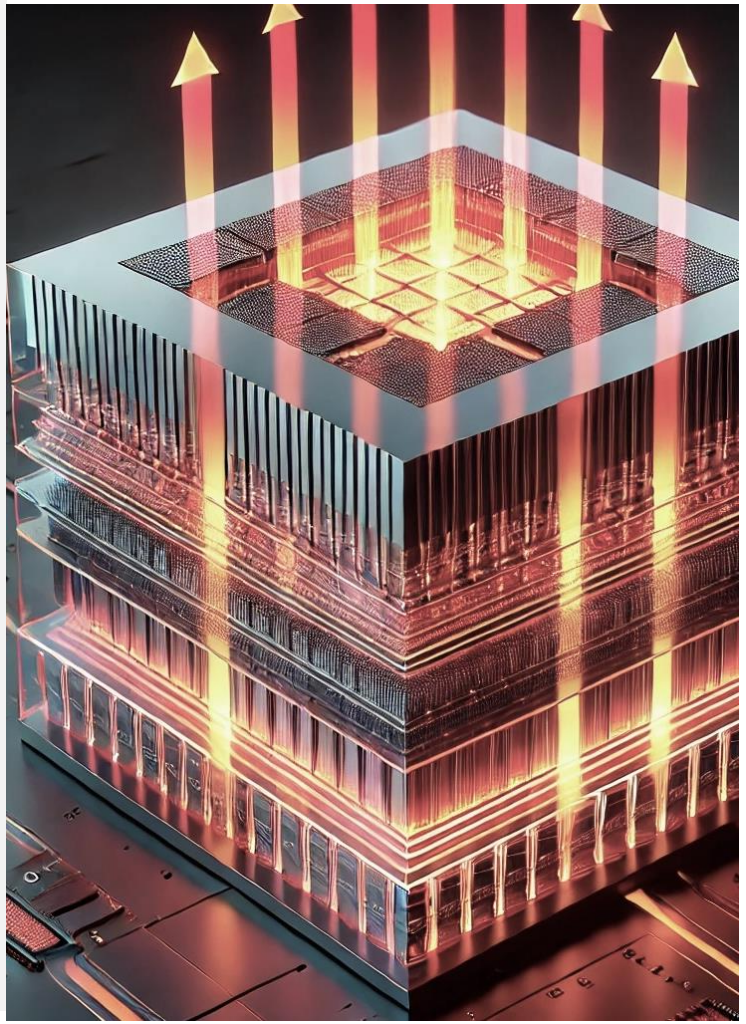
High Power Chips

- Critical element in electrified automobiles
- Thermal power concentrated in narrow device region
- Failure points limit overall voltage/power capabilities
- Lower voltage→ longer charging time, reduced efficiency



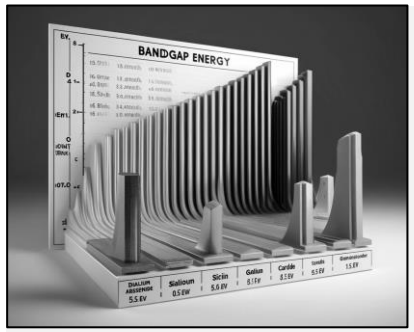
2.5D & 3D Chips

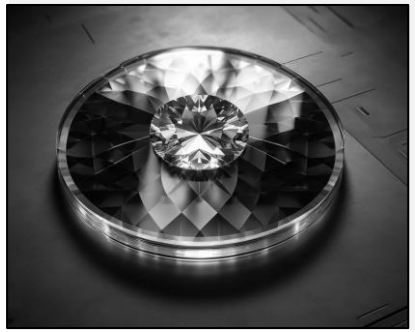
- Modern architecture used in advanced chips
- Allows for higher integration, improved functionality
- Increased thermal challenges
  - Heat transfer between chiplets



WD Advanced Materials

Diamond As An Ultra-Wide Bandgap Semiconductor





The Reason

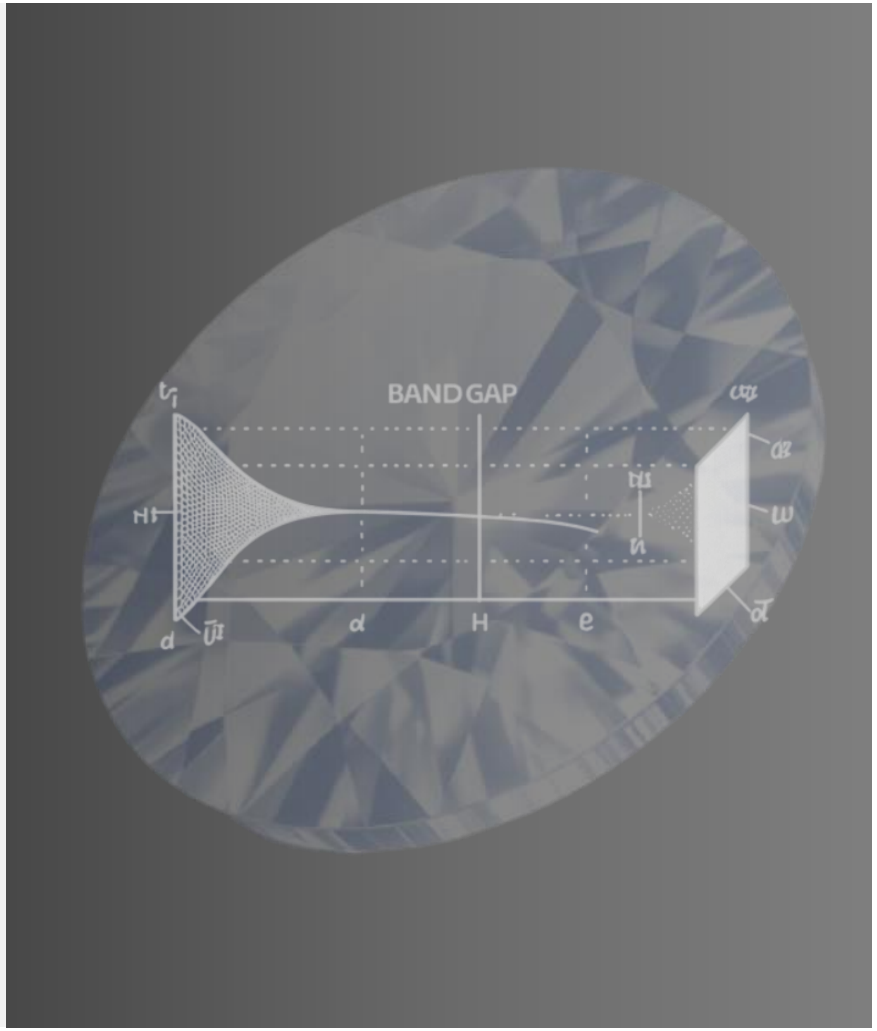
- High electron mobility: 2200 cm^2/Vs
- Thermal conductivity: 2,200 W/(m·K)
- Bandgap: 5.47 eV
- Efficient p-type dopant incorporation

The Challenges

- Current size limitations — typical sizes ~mm
- Challenging n-type dopant incorporation
- Wafering difficulties
- Polishing state of the art → mechanical
- Surface quality → low Ra, high sub-surface damage

The Future

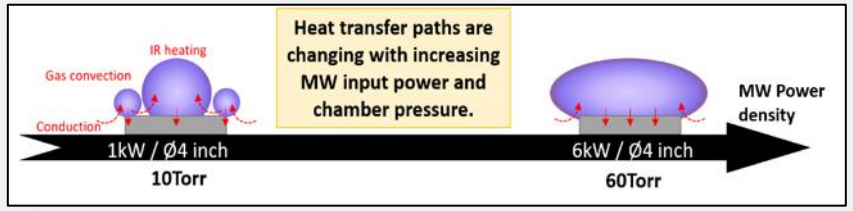
- Polishing solutions already demonstrated
- Cost continues to decline with advancing tech
- DARPA UWBGS → UWGB devices in 3 years
- Heterogenous devices | Simplified thermal

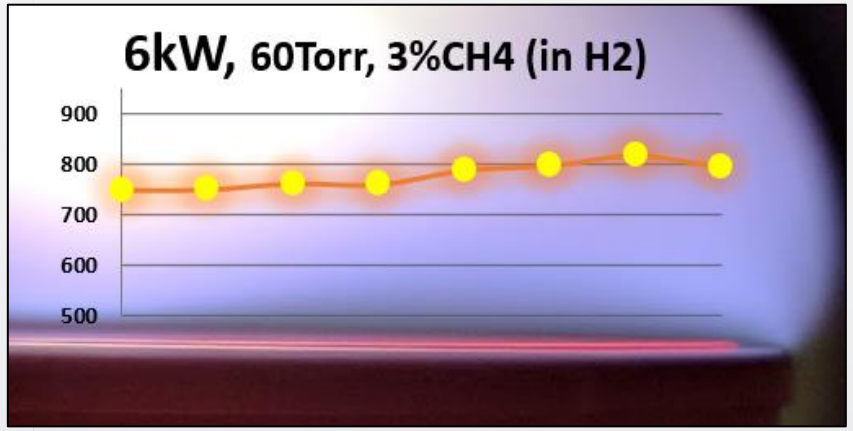


WD Advanced Materials

D100-SCALE — Beyond 2”

- Multiple modified platforms
  - High-throughput 915MHz technology
  - 100mm capable 2.45GHz technology
- Laser-free wafering
  - Graphitization/cleaving process
  - Sacrificial layers
- New polishing technologies
  - Building on D2-SCALE CMP
  - Dry polish finish – atomic scale





UWBGS | D100-SCALE

The Goal

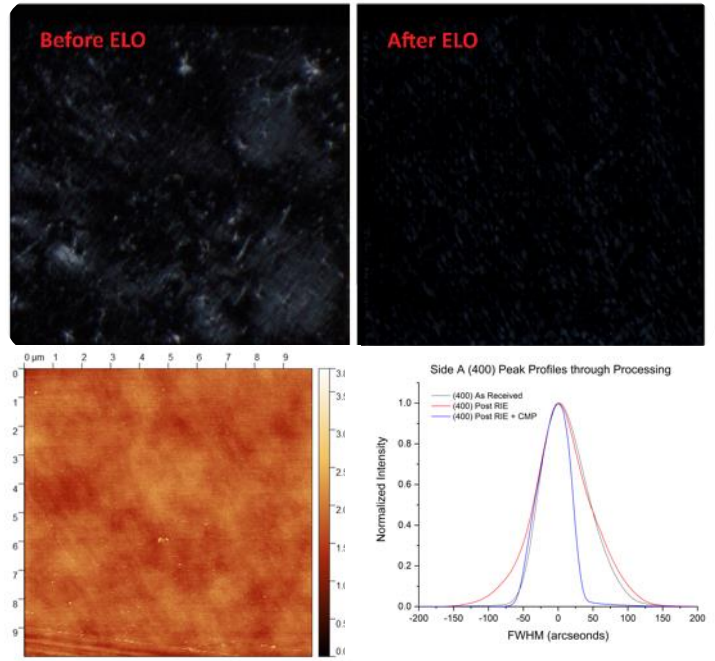
- > 100mm 'device-grade' wafers
- < $10^5/cm^2$ dislocation density
- < 5 x $10^{16}/cm^3$ point defect density
- < 2Å surface Roughness

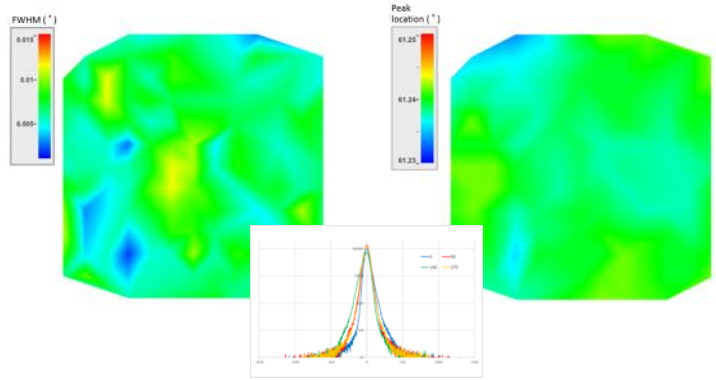
Progress To Date

- Defect mitigation appears to be working as expected
  - Notable stress reduction post-growth
- Optimized polishing results indicate Sa values as low as 1.9Å
  - Indications that 0.8Å is achievable (seen on small samples)
- 38% Reduction in XRD FWHM post polish → elimination of sub-surface damage
- High crystalline quality → ~25 arcseconds typical
- Reduction of FWHM from starting material of >52%

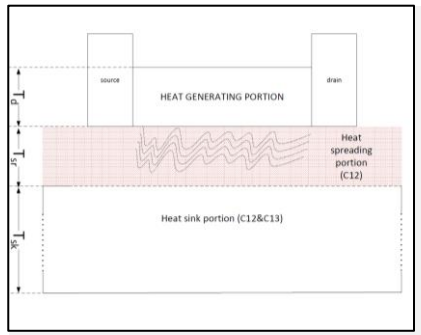
25mm Substrates *Now Available*

- Larger sizes in development



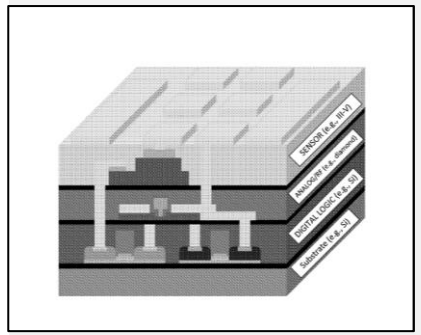


WD Advanced Materials Thermal Solutions



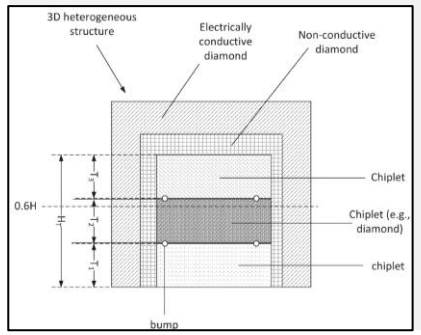
SuperThermal Substrates

- Isotopic enrichment of diamond
  - → 40% increase in thermal conductivity
- Enriched region tuned to device parameters
  - → Similar benefit, reduced cost



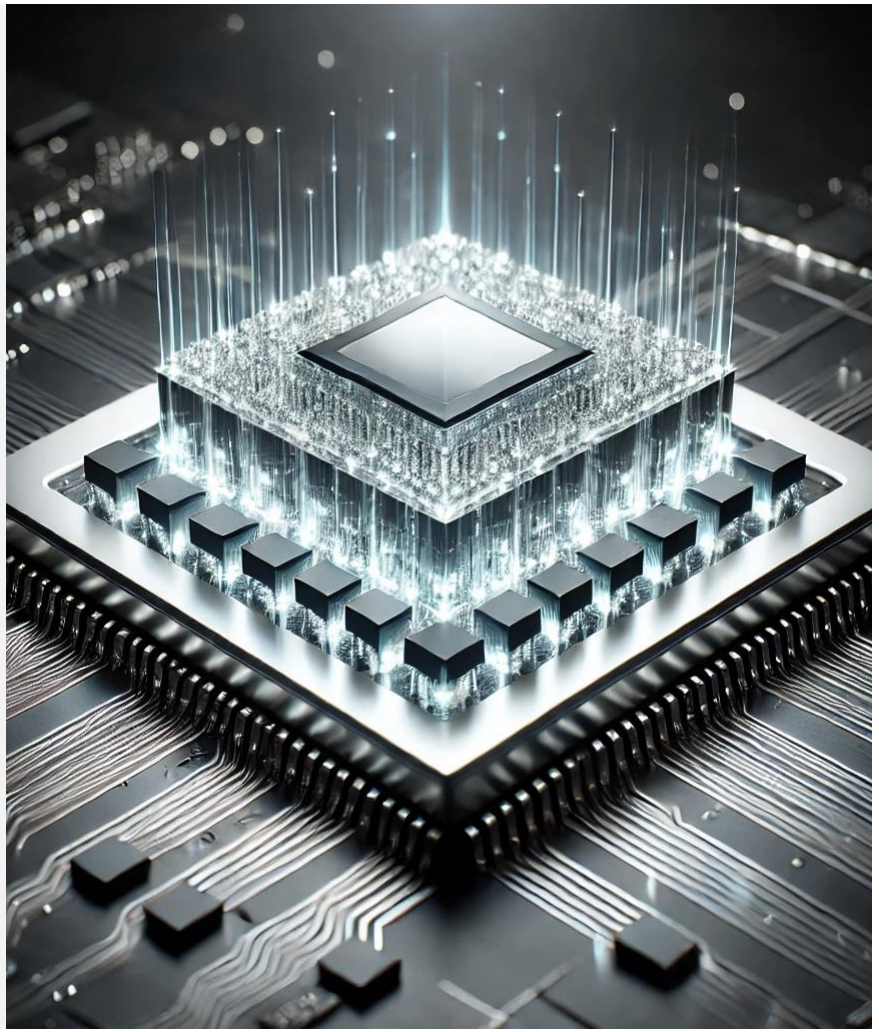
Passive/Active UWBG/Thermal Diamond Chiplets

- Integration of diamond chiplets into device
  - → Power/Frequency applications
- Reduction of intradevice hotspot formation
- Integration with diamond thermal vias



Bimodal Diamond Integration with EMI Protection

- PCD cladding on chip
  - → Pulls heat from chiplet/via to package
- High-κ interface – electrical isolation
- Highly conductive exterior – electrical protection



WD Advanced Materials

WD Advanced Materials

JOHN CIRALDO – Chief Technology Officer
john@wdadvanced.com

For general inquiries: sales@wdadvanced.com
www.wdadvancedmaterials.com