SUNY POLYTECHNIC INSTITUTE

COLLEGE OF NANOSCALE ENGINEERING AND TECHNOLOGY INNOVATION

Faculty Research Report
2016

Michael Carpenter
Interim Dean of the College of Nanoscale Science

College of Nanoscale Engineering Technology Innovation Overview

The College of Nanoscale Engineering and Technology Innovation's (CNETI) was founded in 2014 and encompasses the constellations of Nanoengineering, Nanoeconomics, and Technology and Innovation. The faculty of CNETI are committed to training engineers, entrepreneurs, and leaders capable of developing and commercializing emerging nanotechnologies. CNETI students work with faculty and industry to identify, formulate and solve real-world engineering problems. Through industrial internships and academic research experiences they gain knowledge of cutting-edge technologies and learn the skills and techniques necessary for success in contemporary engineering practice.

CNETI faculty have a record of research excellence in multiple areas including next generation semiconductors and manufacturing, sensor platforms, alternative energy generation and storage, power electronics, and photonics. In addition to the development of new technologies, CNETI has unique expertise in engaging industrial partners to address the manufacturing challenges associated with advanced technologies.

Vision

The College of Nanoscale Engineering and Technology Innovation's (CNETI) vision is to become a premiere world-class institution providing education, training, technology innovation and research experience in nanoengineering, as well as promoting entrepreneurship, innovation, and economic development by leveraging its unique public-private partnerships and resources.

Mission

- Provide an innovative applied learning environment for undergraduate and graduate programs that encompasses integrated research, experimental learning and industry relevance.
- Provide an environment of engineering research excellence that fosters collaborations with internationally recognized organizations including industry, government agencies and other universities addressing societal grand challenges.
- Provide an entrepreneurial ecosystem environment that encourages economic outreach, commercialization of technology and the creation of economic development opportunities.

Constellations

1. Nanoengineering
2. Nanoeconomics / Technology Innovation

Faculty Members

1. **Nanoengineering** – 11 tenure track and 3 adjunct
   Chris Borst, Michael Carpenter (Current Interim Dean), Larry Clow[*], Greg Denbeaux, Harry Efstathiadis, Spyridon Galis, Pradeep Haldar, Ji-Ung Lee, Manisha Rane-Fondacaro[*], Shadi Shahedipour, Woongje Sung, Brad Thiel, Natalya Tokranova[*], Bin Yu
   [*]Adjunct faculty
2. **Nanoeconomics & Technology Innovation** – 3 tenure track faculty (Haldar dual appt. in nanoengineering and nanoeconomics)
   Unni Pillai, Laura Schultz, Pradeep Haldar

Research

2012 - 2017 Active Funding: $15,058,086

   2012-17 Ave. active funding per tenure track faculty: $1,158,314
   Ave. yearly funding per tenure track faculty: $231,662

2016-17 Expenditures (7/1/16 - 6/30/17) $4,467,704

   Tenure track faculty economic development: $3,118,981
   Tenure track faculty research: $1,348,723
   Average research expenditures per tenure track faculty: $103,748

2016-2017 New Funding (grants, contracts) $1,511,488

2016-2017 Publications, presentations, patents
Publications: 72
Presentations: 52
Patents & Technology disclosures: 2

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COLLEGE OF NANOSCALE ENGINEERING AND TECHNOLOGY INNOVATION
Nanoeconomics Constellation

Nanoengineering Constellation

Economics of Nanomanufacturing
(Unni Pillai)

Scope: Modeling and Simulation of Economic Drivers of Technological change

2016 Accomplishments

TOPIC 1: A Model of Diffusion of General Purpose Technologies

Summary: General Purpose Technologies (GPTs) play an important role in economic growth because such technologies give rise to production inputs that are useful across a wide swathe of firms in the economy. Steam engines and semiconductor chips are canonical examples of inputs based on general purpose technologies. GPTs drive output growth through innovations that increase the productivity of inputs based on the technology, and through the diffusion of such inputs across firms in the economy. We develop a parsimonious model of innovation and diffusion of such technologies, building upon the monopolistic competition model in Dixit and Stiglitz (1997).
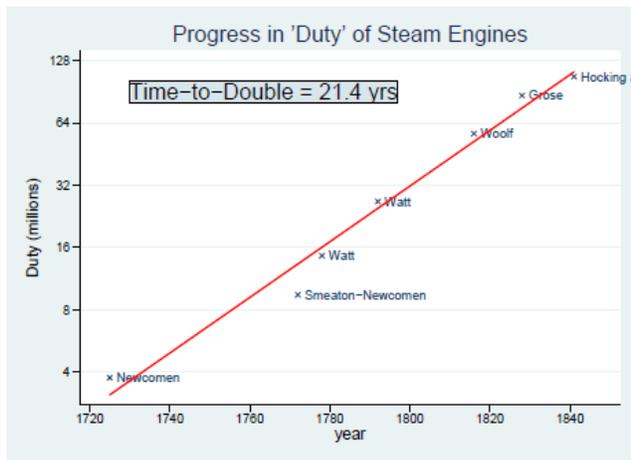

Figure 1: Increase in Duty of Steam Engine.
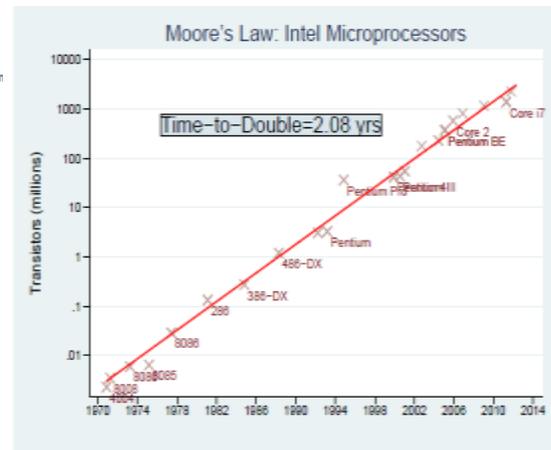
Figure 2: Moore's Law.

TOPIC 2: General Purpose Technologies, Specialization and Output Growth

A long line of economic thought has dwelled on the connections between general purpose technologies, specialization, and output growth. Investigations into these connections to date have proceeded by exploring the linkages between any two of these ideas. In this project, we develop a theory that connects all three and illustrate our theory using a modified version of the monopolistic competition model. The model provides conditions under which generality of input use leads to specialization, and the conditions under which such specialization results in faster output growth.

The key parameter that determines whether specialized suppliers emerge for undertaking the R&D and manufacture of a general purpose input is the coefficient of technological convergence, a summary measure of the level of technical generality of an input. If the coefficient is less than zero, specialized suppliers will emerge and specialization will lead to faster output growth. If coefficient is greater than zero, vertical integration will occur in the long run. Further, if the coefficient is zero then the vertical market structure is governed by considerations in conventional theories, and vertical market structure has no impact on the rate of output growth.

The project will provide useful quantitative model to explore the evolution and growth of nanotechnology, and the role that specialized equipment suppliers play in this growth.

INITIATIVE: New York Business Plan Competition
Dr. Laura Schultz

Scope: The New York Business Plan Competition invited 100 teams to participate in the 8th annual finals on April 28, 2017. 800 students on 331 teams from 59 colleges and universities competed in 10 regional semifinal competitions over the Spring Semester. The top teams from each region advanced to the finals to compete for the $100,000 grand prize.

Goals: The New York Business Plan Competition is a statewide initiative to provide college students with
- **Applied learning-based curriculum and experience in identifying and validating entrepreneurial opportunities**
- **Opportunities to network with top investors and business leaders**
- **Critical seed funding to support collegiate entrepreneurship and technology transfer**
- **Connections to New York's entrepreneurial eco-system**

2016 Accomplishments

- Since 2010 6,500 students on 2,500 teams have participated at statewide events
- 36 of the 532 ventures that have pitched in the NYBPC Finals are still active
- NYBPC ventures have gone on to raise $36.7M in public and private funding after competing
- Each $1 awarded has helped ventures raise another $37.

NYBPC Alumni

INITIATIVE: Building a workforce for emerging technologies
Dr. Laura Schultz

Scope: Understanding the role workforce plays in the successful launch of emerging technologies and advanced technology economic development.

Goals: Survey workforce availability for emerging technologies and identify policies in programs in place to promote technology-based economic development.

2016 Accomplishments

TOPIC 1: Cutting-edge strategies for regional economic development aim to harness and leverage the expertise and resources of universities, industry, and government to generate economic growth. This growth emerges, in part, from a workforce with the skills needed to take up jobs within R&D clusters and to attract new firms in associated sectors to the region. This case study shows how the College of Nanoscale Science and Engineering, led to the transformation of the Capital Region's workforce. It demonstrates CNSE's roles in fostering the development of the nanotechnology workforce at different levels and education skills in response to workforce demand.

Schultz, L., Wagner, A., Gerace, A., Gais, T., Lane, J. and Monteil, L. (2015) "Workforce Development in a Targeted Multisector Economic Strategy" Chapter in Transforming U.S. Workforce Development Policies, eds. Van Horn, Edwards, and Greene. Federal Reserve Bank of Atlanta (2015).

TOPIC 2: Finding appropriate data to track the employment related to emerging technologies and industries is challenging. Federal and state data sources are lagged and often don't have appropriate classifications to observe trends in emerging areas. Professor Schultz partnered with job search engine, Indeed, to see if their "big data" could answer the question. The result was a blog post related to the emergence of renewable energy and environmental employment in the US. The early stage work was highlighted in several news outlets including the Wall Street Journal and Yahoo Finance.
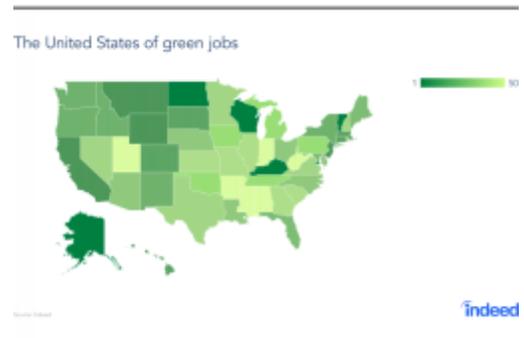
Sinclair, T., and Schultz, L. "The United States of Green Jobs: Where to Find Work Protecting the Environment". Indeed Blog. http://blog.indeed.com/2017/04/19/where-to-find-work-protecting-the-environment/ April 19, 2017

Chemical Sensors
(Carpenter)

Scope: Study the optical, electrochemical and catalytic properties of nanocomposites comprised of plasmonically active metal nanoparticles in metal oxides as a function temperature and gas exposure

Goals: 1) Develop plasmonically active nanocomposites for use as novel functional nanomaterials within harsh environments and 2) Design and develop Si MEMS based electrochemical sensors for harsh environments

2016 Accomplishments

TOPIC 1: Multiwavelength tunability: Multipolar plasmonics

The results detailed in this work illustrate a pathway to improved gas response in plasmonic sensors at high temperatures, which increases the number of plasmonic signatures that can be monitored and serve as beacons for chemical changes in harsh environments. Specifically, higher order plasmonic resonances in large nanoparticles have been exploited to achieve a narrow plasmonic response and for the first time, demonstrate high temperature gas sensing with these higher order modes. The hexapole mode has been identified both experimentally

Figure 1: Plasmon spectra as a function of incident light polarization

and modelled theoretically for 255nm x 60nm gold nanoparticles embedded in YSZ and is shown to follow the same polarization dependence as the longitudinal dipole mode. Due to the 36% decrease in linewidth of the hexapole peak compared to the transverse dipole, the figure of merit (FoM) of the multipolar resonance is calculated to be 22% higher than the longitudinal dipole resonance for the shown gas sensing results and is promising for high temperature gas sensing applications.

TOPIC 2: Development of thermal energy harvesting methods and materials to enhance the integratability and detection properties of harsh environment chemical sensors

The Carpenter group has extended its energy harvesting methods further into the near infrared and have used these properties for the sensitive and selective detection of emission gases under harsh environment conditions.
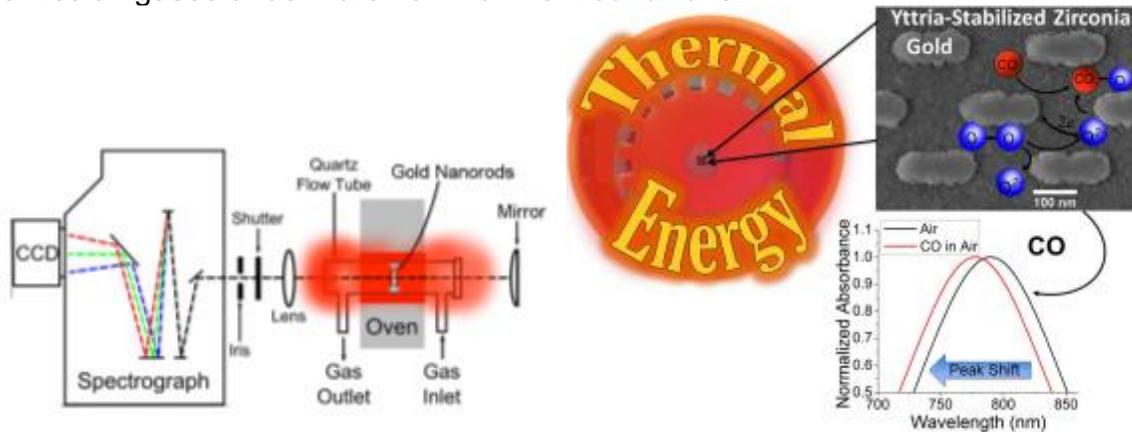

Figure 2: a) Schematic of the thermal imaging bench setup (left). b) Diagram showing the placement of the sample in the Macor holder inside the furnace (right). Interfacial surface reactions between CO and oxygen species are also shown.

The schematic in Figure 2 displays the methods used for this demonstration, which simply require the collection of the thermal energy emitted from the furnace to serve as the background radiation intensity, I_o, for normalizing the intensity of the radiation that passes through the plasmonically active sample, I, and calculation of the associated absorbance spectra. By designing Au nanorods (AuNR) embedded in YSZ, which absorb NIR energy (1400nm) that overlaps with the black body radiation emitted by the furnace operating at 700C, the energy is harvested by the AuNRs and an external incident light is not needed for these experiments. By extending these methods further into the NIR the Carpenter group has improved this methodology such that data collection rates were improved by over an order of magnitude. Chemical sensing tests completed with this newly developed method are comparable to those which use an external incident light source. These results have been critical towards the future development of integratable plasmonics-based sensors in harsh environments and are also expected to be widely applicable for a range of thermal energy harvesting applications, including catalysis.
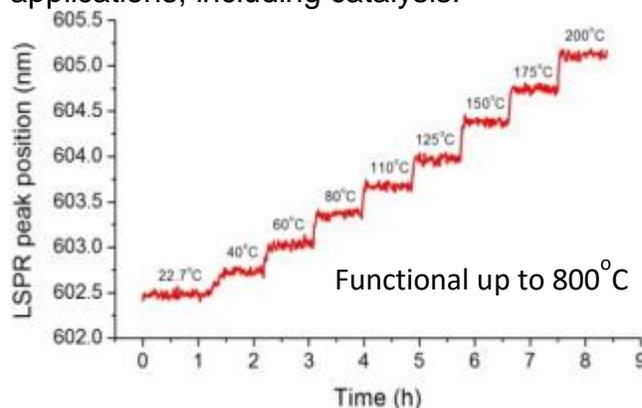

Figure 3: Plasmon peak position as a function of temperature

TOPIC 3: Chemically resistant plasmonic based temperature sensors

Work has been undertaken to develop chemically resistant plasmonic-based temperature sensors. Given that plasmonically active materials are

sensitive to any changes in their surrounding dielectric environment, a plasmonic temperature needs to be impervious to these changes. By embedding the plasmonic particles in either an amorphous SiO_2 layer or a heterostructured design we have shown that these particles can be exposed to acidic/basic solutions as well as high temperature gaseous reactive environments without a change in their plasmonic signature. Furthermore, experiments have shown that given the thermal expansion of the Au nanoparticles crystal lattice the free electron density intrinsically changes as a function of temperature and is the dominant factor over other scattering processes for modifying the plasmonic signature. Acquired data has shown a linear change in the plasmonic peak position as a function of temperature with the melting point of the plasmonic particle being the upper limit of functionality.

TOPIC 4: Design and development of Si MEMS based electrochemical sensors for harsh environments

In partnership with Ohio State University and MicroAdventure Technologies the Carpenter group has continued the development of Si MEMS-based electrochemical sensors. These sensors will be compatible with harsh environments and will target industrial applications including power, transportation and combustion. Oxygen sensors
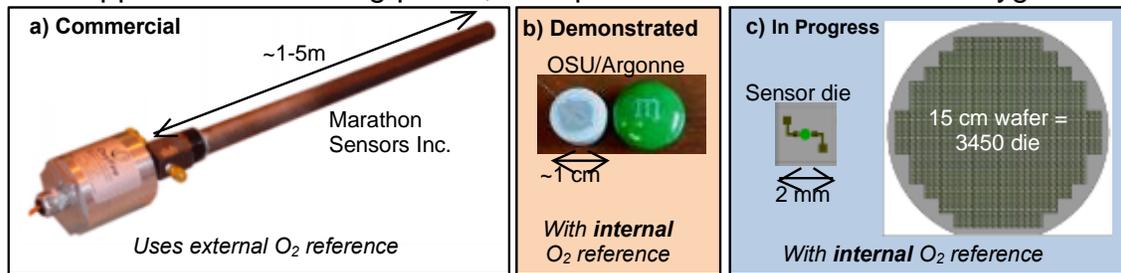

Figure 4: Comparison of scale and designs of industrially available O_2 sensors with the proposed design

are used ubiquitously across these industries to improve efficiency of their respective industrial processes. However, there is a critical need for cost effective miniaturized sensors for better mapping of system conditions, which would increase combustion efficiency, reduce emissions and increase power generation efficiency. Figure 4 outlines the current state of the art in industrially available oxygen sensors, for which these sensors need an external O_2 reference. The MEMS-based design will improve upon a demonstrated ceramic "pellet" based O_2 sensor design which uses an integrated internal O_2 reference and furthermore will enable the fabrication of 3500 sensors on a 6" Si wafer. MEMS fabricated O_2 sensor designs are currently being fabricated using facilities available to SUNY Poly CNSE. Future sensor designs will utilize a plug-n-play type device structure enabling the detection of a suite of gases including O_2, CO, NO_2 and other emission related gases.

Publications
1. J. Elwood, Z. Zhao, L. M. Saupe, T. D. Strayer, R. N. Odell, M. A. Carpenter, "Gold Nanoparticles Embedded in Soda-lime Glass Substrate for Temperature Sensing", Sensing and Biosensing Research, **11**, 37- 44 (2016).
2. Z. Zhao, V. A. Vulcano Rossi, J. P. Baltrus, P. R. Ohodnicki, M. A. Carpenter "Ag Nanoparticles supported on Yttria-stabilized Zicronica: A Synergistic System within Redox Environments", J. Phys. Chem. C, **120**, 5020-32 (2016).
3. Z. Zhao, J. Elwood, M. A. Carpenter, "Phonon Anharmonicity of PdO Studied by Raman Spectrometry", J. Phys. Chem. C, **119,** 23094 (2015).

Presentations
1. M. A. Carpenter, "Thermal Energy Harvesting Plasmonics Based Chemical Sensing", DOE-NETL, 2016, **Invited**
2. M. A. Carpenter, "Chemical Sensors: Use of Dipole and Multipole Plasmonics", Fall 2015 MRS Meeting, **Invited**
3. M. A. Carpenter, "Plasmonics Enabled Chemical Sensors with Thermal Energy Harvesting Attributes", Chemical and Biomolecular Engineering Department, University of Connecticut, Fall 2015, **Invited**

Professor Harry Efstathiadis

Scope: Material deposition and characterization for thin film graphene/CuInGaSe$_2$- and Si-based solar cells, development and evaluation of Si-based nanostructured coatings for solar cells and IR detectors, fabrication and testing of Near InfraRed Reflectors (NIR) as Smart Glass.

Coating development for stainless steel bipolar plates in proton exchange membrane fuel cells (PEMFC).

Solar thermal-electrochemical-photo (STEP) water splitting cell

Goals: Develop and characterize the absorber layer, buffer, transparent conducting layers of CuInGaSe. Replace CdS with graphene and study graphene n-type doping.

Optimize the antireflection properties of SiO$_2$ nanostructures for solar cells.

Develop nitride based film to prevent corrosion of stainless steel bipolar plates used in PEM fuel cells and perform corrosion resistance and electrochemical testing.

Develop a hybrid photoelectrochemical (PEC) water splitting system that dissociates heated water recycling the residual thermal energy produced by a phosphoric acid fuel cell and demonstrate photoanode structures of Diamond/InGaN/Silicon with indium fractions x < 30% that produce hydrogen through water splitting under AM1.5 solar illumination for at least 240 hours

Perform fundamental understanding of materials and processing.

Perform materials composition and device fabrication

2016 Accomplishments
1. G. Pethuraja, J. Zeller, R. Welser, A. Sood, H. Efstathiadis, P. Haldar, P. Wijewarnasuriya, and N. Dhar, Development of Nanostructured Antireflection Coatings for Electro-Optic Infrared Technologies, submitted to Sensors & Transducers (2017).
2. Ashok K. Sood, John W. Zeller, and Yash R. Puri, Caitlin Rouse, Pradeep Haldar, and Harry Efstathiadis, Nibir K. Dhar, Priyalal S. Wijewarnasuriya, "SiGe Focal Plane Array Detector Technology for Near-Infrared Imaging", submitted to International Research Publication (2017).
3. J. Warrender, Q. Hudspeth, G. Malladi, H. Efstathiadis and J. Mathews, "Incorporation of gold into silicon by thin film deposition and pulsed laser melting", Applied Physics Letters 109, 23 (2017).
4. J. Claypoole, M. Altwerger, D. Dwyer, S. Novak, P. Haldar, M. Eisaman, H. Efstathiadis, "Sputter Rate Measurements of Cu(In,Ga)Se$_2$ Absorber Layers with

Varied Ga Ratios, Primary Voltage, and Angle of Incidence by Secondary Ion Mass Spectrometry", Journal of Alloys and Compounds 696, 808–813 (2017).

5. J. Zeller, C. Rouse, H. Efstathiadis, P. Haldar, J. Lewis, N. Dhar, P. Wijewarnasuriya, Y. Puri, A. Sood, "Development of silicon-germanium visible-near infrared arrays", Proc. of SPIE Vol. 9854 985408-1 (2016).

6. G. Pethuraja, R. Welser A. Sood, H. Efstathiadis P. Haldar, P. Wijewarnasuriya, N. Dhar "Development of Nanostructure Antireflection Coatings for EO/IR Sensor Applications", Proc. of SPIE 9854 985407-1 (2016).

7. A. Sood, I. Lund, J. Zeller, Y Puri, H. Efstathiadis, P. Haldar, N. Dhar, J. Lewis, P. Wijewarnasuriya, "Development of Graphene Based Detectors for EO/IR Applications", Proc. of SPIE 9854 98540D-1 (2016).

8. C. Rouse, J. Zeller, H. Efstathiadis, P. Haldar, J. Lewis, N. Dhar, P. Wijewarnasuriya, Y. Puri, A. Sood, "Development of Low Dark Current SiGe Near-Infrared PIN Photodetectors on 300 mm Silicon Wafers", Optics and Photonics Journal, 6, 61-68 (2016).

9. R. LaForest, I. Gherasoiu, D. White, and H. Efstathiadis, "P-TECH: A New Model for an Integrated Engineering Technology Education", Proc. of St. Lawrence Section of the American Society for Engineering Education, (2016).

10. D. Dissanayake, A. Ashraf, D. Dwyer, K. Kisslinger, L. Zhang, Y. Pang, H. Efstathiadis, and M. Eisaman, "A Scalable, In situ and Spontaneously n-Doped Graphene Schottky Diode", *Nature Scientific Reports,* 6, 21070 (2016).

11. B. Peace, J. Claypoole, N. Sun, D. Dwyer, M. Eisaman, P. Haldar, and H. Efstathiadis, "Characterization of Cu(In,Ga)Se$_2$ (CIGS) films with varying gallium ratios for thin-film photovoltaic (PV) devices", Journal of Alloys and Compounds 657, 873-877 (2016).

TOPIC 1: Solar Cells
N-type Graphene Doping with Alkali Fluoride Post deposition treatments

Copper indium gallium di-selenide (CIGS) thin film solar cells have demonstrated lab scale efficiencies comparable to polyctystalline silicon cells. The buffer layer of CIGS devices, which is the CdS, is usually deposited by a chemical bath deposition (CBD). In this work, we are working to replace CdS with graphene and also demonstrate graphene n-type graphene doping. Doping of graphene could also improve technologies in many technologies, such as microelectronics, optoelectronics, and energy storage. While high p-doping has been demonstrated, n-type doping of graphene with electron densities above 10^{12} e/cm^2 is difficult to achieve. We have demonstrated high n-type doping graphene on a soda-lime-glass substrate via surface-transfer doping from Na. The n-type doping reaches 2.11 × 1013 e/cm^2 when graphene is transferred onto a p-type CIGS semiconductor that itself has been deposited onto soda-lime-glass, via surface-transfer doping from Na atoms that diffuse to the CIGS surface.
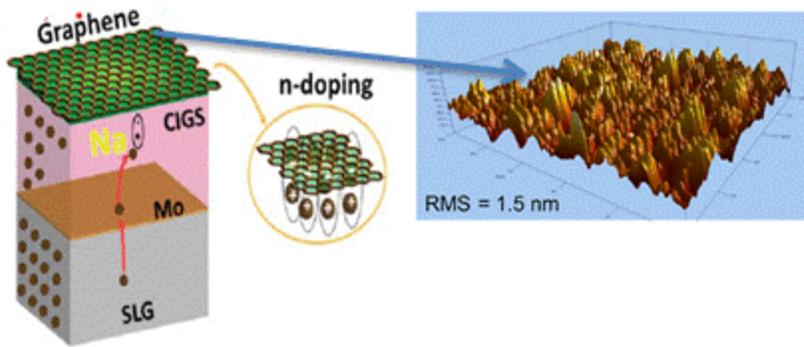
Figure 1: Eliminated the use of CdS as buffer layer and replaced it with graphene. The n-doping reaches 2.11×10^{13} e/cm^2 when graphene is transferred onto a p-type CIGS deposited onto soda lime glass.

Large-Area Nanostructured Self-Assembled Antireflection Coatings for solar cells and optical devices

A variety of transparent protective sheets such as glass and polymers have been used for photovoltaic (PV) modules. The work was performed on CIGS devices but can also be used in Si-based solar cells and also applied to IR detectors or optical devices. The light propagating from the air into the protective sheet undergoes unwanted Fresnel reflection at the air/sheet interface due to the dissimilar optical properties of the media. Although Fresnel reflection losses are relatively low at normal incidence, they can become quite substantial for off-angle light incidence. For example, Fresnel reflection at an uncoated glass/air interface generally varies from over 4% at normal incidence to more than 40% at a 75° incident angle. The Fresnel reflection limits the amount of light transmitted to the underlying energy harvesting device. Minimizing the reflection losses increases the density of photo-generated carriers, resulting in an enhancement of module efficiency.

Oblique-angle deposition is a method of growing porous thin films, and hence thin films with low-refractive index enabled by surface diffusion and self-shadowing effects during the deposition process. Figure 1 shows the experimental setup used in the oblique-angle deposition technique for growing porous nanostructured materials.
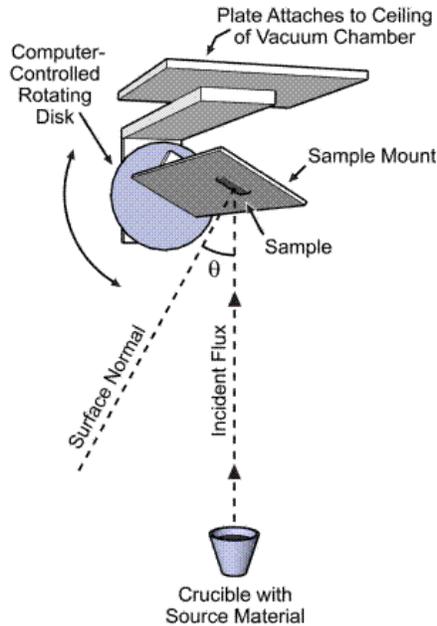
Figure 1: Illustration of the experimental setup used in the oblique-angle deposition technique for porous nanostructured materials. The incident physical vapor flux strikes the sample at an angle relative to the surface normal.

In this work, antireflection (AR) coatings with specular surfaces comprised of multiple layers of porous SiO_2 layers have been deposited on 6-inch glass wafers. The specific target thickness and refractive index values for the step-graded structure were chosen to minimize an unwanted dip in transmittance near 550 nm due to interference effects. Double-sided structures were prepared in an electron-beam evaporator using a multi-step process that included two or three different deposition angles and two-step deposition at each angle. Figure 2 shows a cross-sectional scanning electron micrograph of typical porous nano-material thin-films grown by oblique-angle deposition using silicon dioxide.
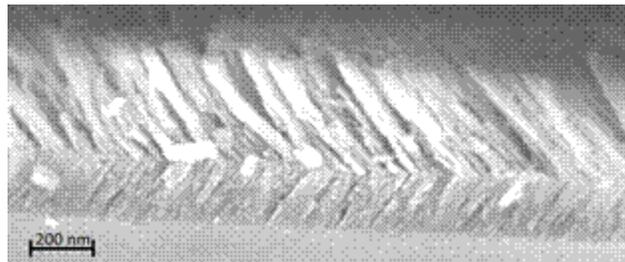
Figure 2: Cross-sectional scanning electron image of a multi-layered nanostructured of SiO_2.

To confirm the antireflective characteristics of the large area AR coating, light from a solar simulator was transmitted through both an AR-coated and an uncoated glass wafer, and analyzed using a CIGS thin-film-based PV device. Light transmitted through the AR-coated glass wafer yields 5% more short circuit current compared to light transmitted through the uncoated glass wafer at normal light incidence. This is illustrated in Figure 3.
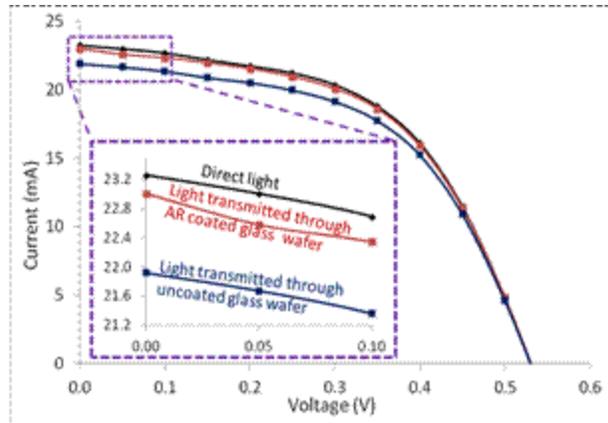
Figure 3: Current-voltage characteristics of a CIGS photovoltaic device under illumination of direct light, as well as light transmitted through an AR-coated glass wafer and light transmitted through an uncoated glass wafer.

## Sputter Rate Measurements of Cu(In,Ga)Se₂ Absorber Layers with Varied Ga Ratios, Primary Voltage, and Angle of Incidence by Secondary Ion Mass Spectrometry

Thin film $Cu(In,Ga)Se_2$ layers were deposited by a 1-stage and 3-stage co-evaporation process on Mo/Glass substrates at various Ga/(Ga+In) ratios (Ga ratio). The sputter rate and the depth profile of 1-stage CIGS absorber layers at various Ga ratios were measured using secondary ion mass spectrometry (SIMS) using different primary voltages and angles of incidence of a Cs beam in order to study how the Ga ratio of CIGS affected the sputter rate. It was determined that there was up to 50% variation in film sputter rate depending on the Ga ratio range, SIMS primary voltage, and angle of incidence. A point-by-point correction method was then developed to correct for relative sputter rate differences in 3-stage CIGS samples with a graded Ga ratio profile. We have shown how the sputter rate of 1-stage CIGS absorber layers with Ga ratios between 0 and 0.5, primary Cs beam voltages between 2-5 kV, and angles of incidence of 45 and 60 degrees affect the sputter rate. It also demonstrates a point-by-point correction of a graded CIGS absorber layer based on Ga ratio.

Light Redirection in Optoelectronic Devices Through Self-Aligned Vertical

The combination of anti-reflection coatings (ARCs) with surface texturization is the standard industrial practice for preventing optical reflection losses in crystalline silicon (c-Si) photovoltaics. However, the operating mechanism of this approach is governed by Snell's Law, which places a limitation on the maximum transmission angle of incident radiation. We have developed a novel light trapping concept that utilizes a nanoaperture array to reduce both broadband and high angle reflections, while increasing the optical transmission angle beyond that dictated by Snell's Law. Our investigation seeks to demonstrate an increase in photovoltaic device efficiencies through optical manipulation of incident light by a fabricated nanoaperture array. We are working to develop a fabrication process for solar devices with and without nanoaperture arrays using conventional microelectronics techniques. P/n junction formation was completed using

ion implantation and annealing. Lithography and reactive ion etching was used to create nanoaperture arrays in an ARC coating.

The fabrication of a 2D nanoscale grating incorporated into the passivation/anti-reflection layer to improve the light trapping efficiency of the solar cell can be accomplished in several ways. In this effort, the solar cell was fabricated in the CNSE 300mm fabrication facility using a 300mm p-type boron doped (100) Si wafer (specified as 1-10 ohm-cm resistivity) as the substrate. To create the grating structure, the ARC deposited on the solar cell device. A 193nm lithography resist stack was then exposed through the 193nm immersion lithography tool (ASML) to create an array of 1 dimensional gratings shown in Fig 1 below.
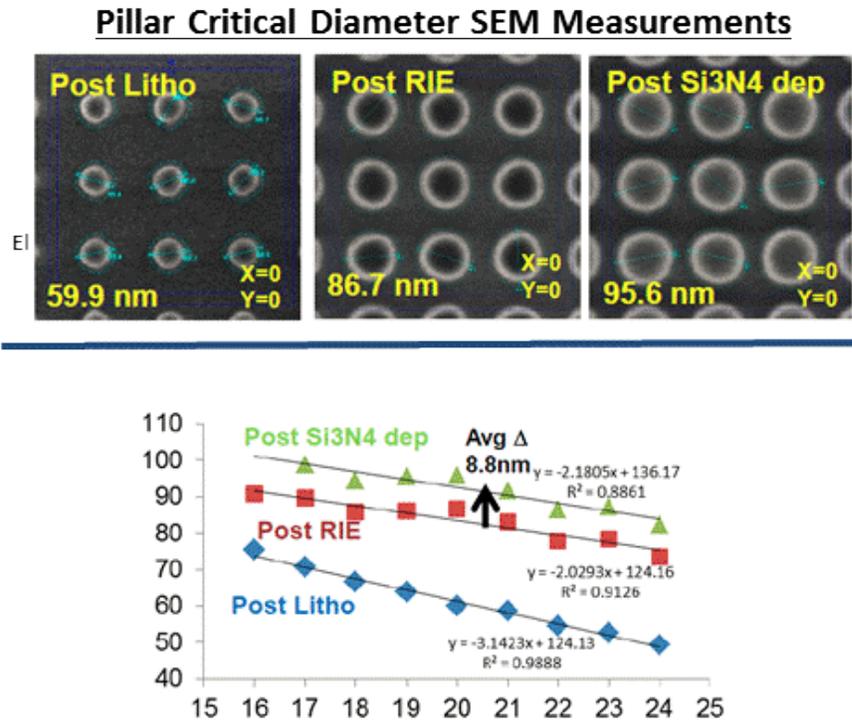

Figure 1: SEM micrographs illustrate how dual exposures created a 2D array of resist pillars of varying diameters. Towards the higher extreme of the lithographic process budget, the features began to coalesce into each other. The diameter of the ARC pillars post RIE was measured as a function of dose for each of the nine areas.

Near InfraRed Reflectors (NIR) as Smart Glass*

Solar panels are ensembles of solar cells that convert solar light into electricity. During the day, the temperature of the solar panel can reach as much as 90°C. With each degree centigrade the conversion efficiency of the solar generator decreases by 0.46%. Thus, on a hot summer day, the power generated can decrease by almost 30%. Moreover, the amount of energy that is spent annually for thermal conditioning of the buildings in the United States is more than 400 billion kilowatt-hours, according to the

U.S. Energy Information Administration and the windows are the surfaces that enable the wasteful heat exchange.

Therefore, the development of a versatile and robust metamaterial that can reflect near infrared heat radiation (NIR) in the range 0.7-2.5 µm while transmitting more than 90% of the visible light intensity is highly desirable. Metal oxides can be used to manage the light reflectance over the long wavelength range. However, to obtain high reflectivity starting at shorter wavelengths, the doping concentration of the metal oxide has to be increased above the level of $1x10^{21}/cm^3$. At these concentrations, the dopant incorporates not only substitutionally but large amounts will also be found interstitially. Interstitial dopants have been shown to produce carriers with heavier effective mass, decreased mobility, and deeper donor states that significantly decrease the transmittance. Ultimately substitutional dopants degrade the crystallinity of the host material, generating compensating defects that limit the achievable carrier density.

To circumvent the need for excessive dopant incorporation we propose a structure that alternates insulating and conducting layers of silicon dioxide (SiO_2) and silicon doped zinc oxide film (ZnO:Si). This structure is deposited by magnetron sputtering from Si and ZnO targets at low temperature. The structure uses the electric-field enhancement of carrier density to regulate the bandwidth of the NIR and in turn the amount of heat reflected. This is achieved through the formation of a quasi 2-dimensional electron gas in a thin layer at the dielectric/ZnO:Si interface. Overall the technology could be used in many applications, from the passive reduction of heating on solar cells, to the reduction of the cooling demands in buildings and cars, as well as in the field of photonics.

TOPIC 2: Fuel Cells and Hydrogen Production
Development of Enhanced Titanium Nitride-based Coatings for Stainless Steel Bipolar Plates in PEM Fuel Cells

High cost and short lifetime are the two main reasons why the PEM fuel cell (PEMFC) has not reached a widespread, disruptive level of commercialization. The conventional graphite bipolar plates in a PEMFC are alone responsible for about 45% of the cost and 85% of the total weight of a single cell. Stainless steel has been suggested as the replacement material for new age bipolar plates. The main drawback of using stainless steel as the bipolar plate material is the non-conductive metal oxide film that forms on the stainless-steel surface in oxidizing acidic environments such as that of the PEMFC. This insulating metal oxide layer creates a high contact resistance between successive cells in a fuel cell stack which severely degrades the electrical performance of the device. To prevent this failure mechanism, the stainless-steel surface must be modified to protect against non-conductive oxide formation. The most cost-effective surface treatments in the available literature are physical vapor deposition (PVD) coatings of transition metal nitrides which show much better performance as bipolar plates than uncoated stainless steel, but there is much work to do to minimize coating defects that currently prevent these coatings from being mature enough for widespread commercial use.

The objective of this work is to illuminate specific improvements made by incorporating a thin, pure-metal adhesion layer to transition metal nitride coatings deposited by physical vapor deposition (PVD) on stainless steel substrates for use as bipolar plates in PEM fuel cells. We first examine techniques of characterizing coatings for bipolar plates before using popular titanium nitride (TiN) coatings as a case study. Corrosion tests were performed in H_2SO_4 electrolyte with a pH close to 3 and temperature near 70°C to mimic PEM fuel cell operating conditions with and without different commercial and TiN based coatings; this survey allows for controlled and direct comparison of coatings. Before and after each test, Scanning Electron Microscope (SEM) images, 4-Point Probe (4PP) material resistivity, Interfacial Contact Resistance (ICR), Water Contact Angle (WCA) hydrophobicity, and Inductively Coupled Plasma – Mass Spectrometry (ICP-MS) techniques were utilized to evaluate coating performance as a PEMFC corrosion-inhibitor in the context of relevant characteristic targets for bipolar plate application as listed by the Department of Energy as well as the performance of commercially available corrosion coatings.

Solar thermal-electrochemical-photo (STEP) water splitting cell*

The water electrolysis has an efficiency of ~62% calculated including the losses due to the proton exchange membrane, electrode and interfacial resistances. If solar light is the source of energy than the average PV array could convert the light into electricity with an efficiency of ~17%. Thus, the combined efficiency of the PV-electrolysis system would be of just ~10.5%. Photoelectrochemical (PEC) water splitting has the potential to produce hydrogen through a more efficient process than the photovoltaic (PV) conversion followed by electrolysis. A PEC water splitting process converts solar photons into electron-hole pairs to generate the water splitting potential directly at the semiconductor-liquid interface. A solar PEC consists of semiconductor film with one surface in contact with electrolyte. The other surface is connected to a metallic counter electrode immersed in the same electrolyte. The water dissociation process occurs when the polar covalent bond of the water molecule is broken.

PEC cells with a Solar-to-Hydrogen (STH) efficiency of 18.3% at laboratory scale have already been reported. The proliferation of the technology at the commercial scale has been prevented by the short lifetime of the photoelectrode, the operation of which degrades over the timespan of a few hours.

The proof of concept that we are working on distinguishes it from the previous solutions through the engineering of the energy bands of the "window" and absorber layers, such that they will be properly aligned for the carrier transport over material interfaces and the interface with water (Fig. 1 below). Moreover, the solar-transparent "window" material is relatively immune to the electrolysis corrosion and protects a simple and efficient absorber film with a Solar-to-Hydrogen theoretical efficiency of more than 20%. The semiconductor films will be synthesized using industry accepted chemical vapor deposition tools and methods.

The uniqueness of the design consists of the use of an electrochemically stable boron/phosphorus **co-doped diamond (BPDD) window layer** over an efficient **tandem absorber** layer ($In_xGa_{1-x}N$/Si) with properly tailored band gap (1.8eV) to provide a current match for the silicon solar cell underneath (17.1mA/cm^2). The operation will enable hydrogen generation through water splitting under solar illumination under an average current density in the range from 3 mA/cm^2 to 17 mA/cm^2.
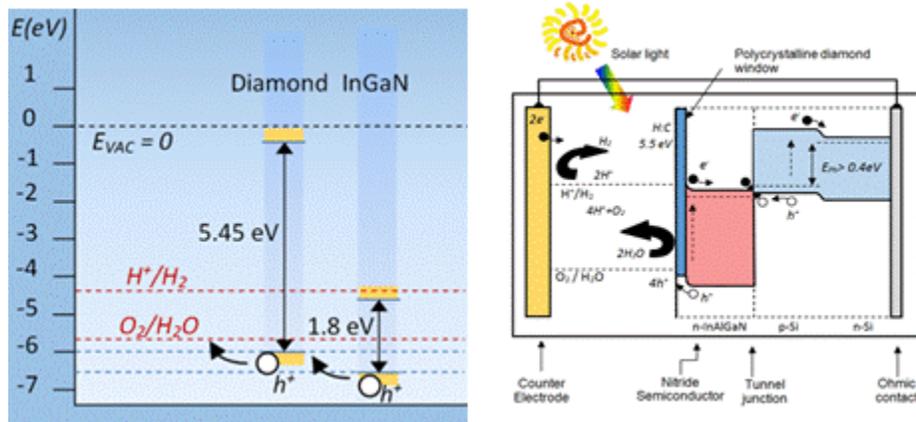

Figure 1: Optimal alignment of semiconductors valence band and water oxidation potential. Photoelectrochemical water splitting system. The semiconductor photoanode at the left is composed of an InAlGaN absorber and a silicon pn-junction subcell. Short wavelength solar light is absorbed by the InAlGaN film while the long wavelength light is absorbed by the silicon cell. The back of the silicon subcell is connected to a platinum counter electrode. Both electrodes are immersed in an aqueous electrolyte.

The structure operation with the addition of a doped-diamond window is based on the transport of the photo-generated holes through suitable VBE alignment: VBE_{InGaN} (6.6eV)→VBE_{BPDD} (6eV)→O_2/H_2O (5.73eV). The buildup of a potential of 0.6 V, across the Si p/n junction, positions the electrons at CBE slightly over the reduction potential of H^+/H_2 in the water splitting process.

Endnotes

*In collaboration with Prof. I Gherasiou from SUNY Poly Utica Campus

Gallis: SGNano Research Group

Goal: Synthesis and characterization of nanostructured materials, SiC nanowires, generation and characterization of color centers in SiC nanostructures for quantum applications, layered semiconductor materials.

Our research aim is to advance the scientific foundation that underlies the current and potential future of materials science. To this end, our research focus is the synthesis, fabrication, and characterization of nanostructured systems for quantum, optoelectronic, and biosensing applications. This direction involves the design and development of novel integration schemes that would allow the synthesis of multifunctional nanostructured materials with predetermined geometries. Another research emphasis is the development of ultrathin silicon carbide (SiC) nanowires (NW) that could be grown in a self-aligned manner in precise locations through an innovative CVD-synthesis route for quantum and NW-biosensing technologies. Concurrently, my semiconductor-related research interests are in the synthesis and characterization of novel layered materials (2D materials).

2016 accomplishments

TOPIC 1: Time-resolved analysis of the white photoluminescence from chemically synthesized SiC_xO_y thin films and nanowires
(Paper published in Applied Physics Letters)[i]

The study reported presents results on the room-temperature photoluminescence (PL) dynamics of chemically-synthesized $SiC_xO_{y \leq 1.6}$ (0.19<x<0.6) thin films and corresponding nanowire (NW) arrays. The PL decay transients of the SiC_xO_y films/NWs are characterized by fast luminescence decay lifetimes that span in the range of 350 – 950 ps, as determined from their deconvoluted PL decay spectra and their stretched-exponential recombination behavior. Complementary steady-state PL emission peak studies for SiC_xO_y thin films with varying C content showed similar characteristics pertaining to the variation of their emission peak position with respect to the excitation photon energy. A nearly monotonic increase of the PL energy emission peak, before reaching an energy plateau, was observed with increasing excitation energy. This behavior suggests that band-tail states, related to C-Si/Si-O-C bonding, play a prominent role in the recombination of photo-generated carriers in SiC_xO_y. Furthermore, the PL lifetime behavior of the SiC_xO_y thin films and their NWs was analyzed with respect to their luminescence emission energy. An emission-energy-dependent lifetime was observed, as a result of the modulation of their band-tail states statistics with varying C content and with the reduced dimensionality of the NWs (Fig. 1).

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[i] Natasha Tabassum, Vasileios Nikas, Brian Ford, Mengbing Huang, Alain E. Kaloyeros and Spyros Gallis: Time-resolved analysis of the white photoluminescence from chemically synthesized SiC_xO_y thin films and nanowires. App. Phys. Let. **109**, 043104 (2016).
http://aip.scitation.org/doi/abs/10.1063/1.4959834?journalCode=apl
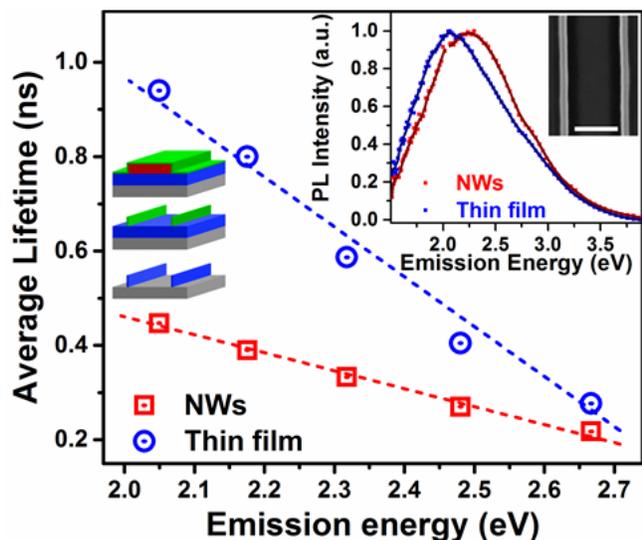
Figure 1: The average lifetimes of the $SiC_{0.34}O_{1.52}$ (12 at.% C) NWs array and its thin film counterpart at different PL emission energies; schematic representation of the SiC_xO_y NWs array fabrication via SIT utilizing SiC hardmask (green) and anisotropic RIE of SiC_xO_y thin film (blue). Inset: Ensemble steady-state normalized PL spectrum of the SiC_xO_y NWs array along with the normalized PL spectrum of its thin film analogue under 4.1 eV excitation. (PL peak position difference: ΔE= ~0.2 eV). Top-down SEM image of SiC_xO_y NWs, scale bar is 200 nm.

TOPIC 2: Silicon Oxycarbide Thin films and Nanostructures: Synthesis, Properties and Applications
(**_Book Chapter_**)[ii]

Silicon-oxycarbide (SiC_xO_y) has been extensively investigated due to its wide use in the Si semiconductor industry in applications that include low-k dielectrics, passivation layers, and etch-stop layers. Furthermore, SiC_xO_y research has been exploring its prospective use in a numerous other technological usages, such as lighting, energy, and biological applications. The latter include white light emitting materials, hydrogen storage materials, gas sensors, anode materials for lithium batteries, and biomedical devices. SiC_xO_y materials can produce intense luminescence in a broad emission spectral range that spans the ultraviolet, the visible and even the near-infrared spectrum when doped with erbium. Herein, we present pertinent results on the material behaviors from chemically synthesized SiC_xO_y thin films and nanowires. Moreover, their light emitting properties and underlying mechanisms for light emission were explored in conjunction with data from their thin films counterparts, which were also employed as baseline comparison metric. We further highlight major challenges and promises of such materials.

TOPIC 3: Realization of Self-Aligned Erbium-Doped Silicon-Carbide Nanowires towards Quantum Technologies
AVS Hudson Mohawk Chapter Fall Meeting - _Awarded as best graduate oral presentation_

[ii] _InTech_, (2017). doi:10.5772/66992

Ji Ung Lee

Scope: Nanoscale device and quantum transport measurements

Goals: Fabricate and characterize nanostructured materials and devices for post-CMOS, energy, and DOD applications. We carbon nanotubes and 2D materials, including graphene and TMD films. To support the experimental efforts, we also perform advanced quantum transport simulations.

2016-17 Accomplishments

TOPIC 1: 3-in-1: Reconfigurable device in 2D Transition dichalcogenide semiconductors

Figure:
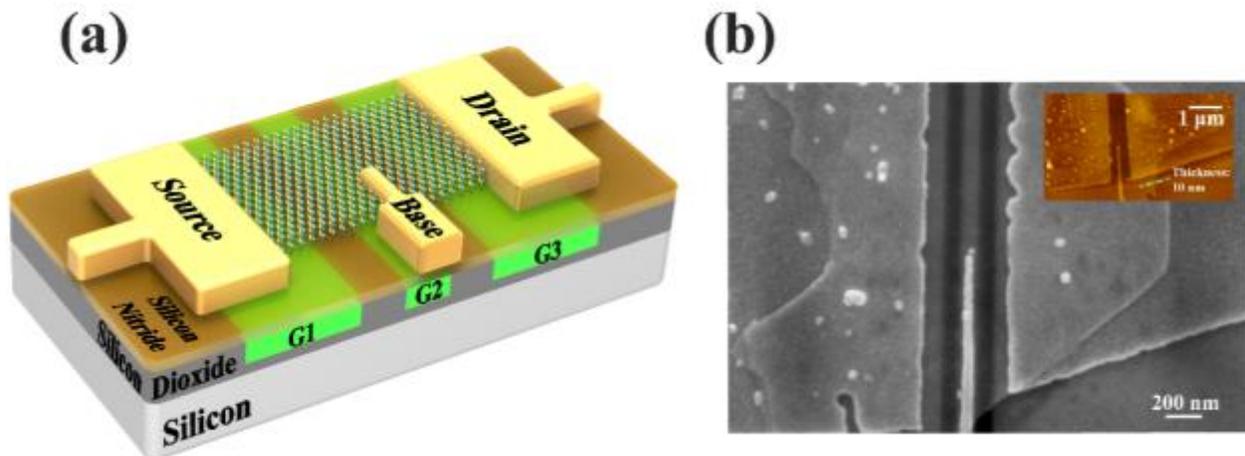
A single device that can function as a p-n diode, a MOSFET, and a BJT: (a) A Schematic of a reconfigurable device with buried gates labeled G1, G2, and G3. They can be biased independently to create an n- or a p-type region within a single WSe_2 flake. The Source and Drain contacts are placed at the two ends of the WSe_2 flake, and a thin Base contacts the edge of the flake. (b) A SEM image showing the buried gates and the WSe_2 flake. The inset shows an AFM image of the device and the green dotted line shows that the WSe_2 is 10nm thick.

Footnote

Published in Nanotechnology and picked up by several news outlets:

Three fundamental devices in one: a reconfigurable multifunctional device in two-dimensional WSe2, P. Dhakra, P. Agnihotri, and J.U. Lee, Nanotechnology 28, 265203 (2017).

Featured in

TOPIC 2: Quantum Transport Modeling of Magnetic Focusing in Graphene p-n Junctions

Figure:
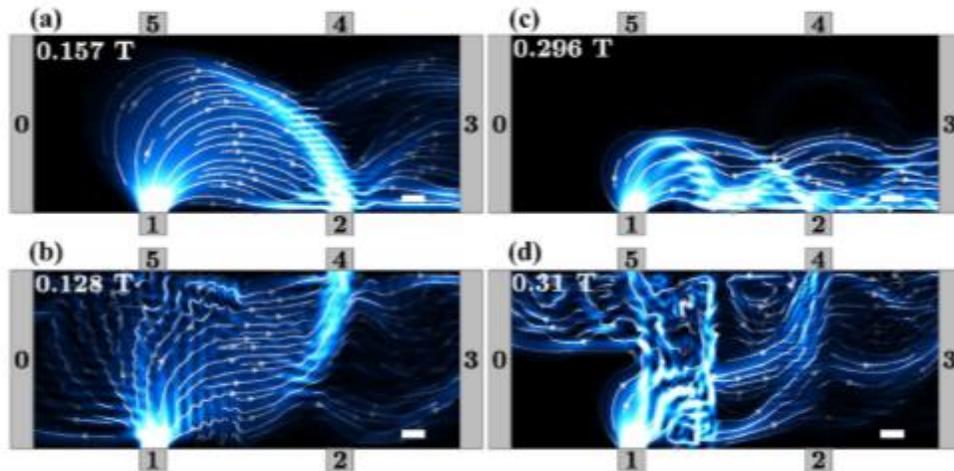
Modeling of electron trajectories in different magnetic fields for a unipolar (a) and (c), and an ambipolar (b) and (d) graphene devices.

Footnote

Understanding magnetic focusing in graphene p-n junctions through quantum modeling, S.W. LaGasse and Ji Ung Lee, Phys. Rev. B 95, 155433 (2017).

TOPIC 3: Radhard Electronics

Figure 1:

(a)

(b)
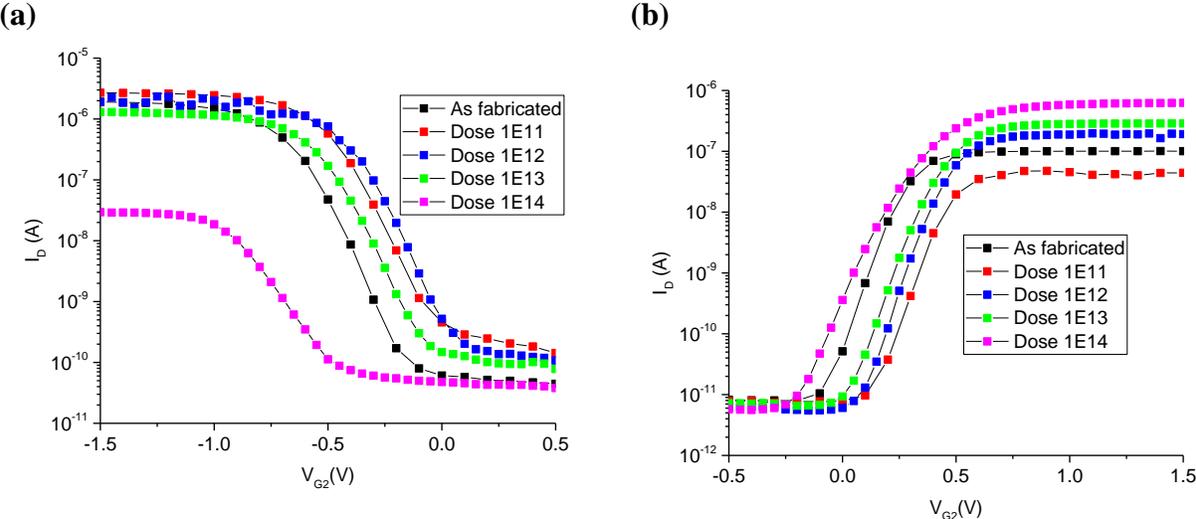
Transfer curves from a single reconfigurable MOSFET device under proton radiation. The device is fabricated using a 2D TMD WSe2 and can reconfigure into both p- and n-channel MOSFETs.

Footnote
Publication submitted

Power Semiconductor Devices
(Woongje Sung)

Scope: Design, fabrication and characterization of wide bandgap power semiconductor devices

Goals: 1) Develop efficient, rugged, and reliable power semiconductor devices, 2) Develop low-cost, reliable, repeatable process baseline to fabricate SiC devices, 3) Develop next generation power devices on novel materials such as homogeneous GaN and Ga_2O_3.

2016 Accomplishments

TOPIC 1: Design and Economic Considerations to Achieve the Price Parity of SiC MOSFETs with Silicon IGBTs [1, 2]

In 2015, U.S Department of Energy has launched an Institute (PowerAmerica) under the initiative of National Network of Manufacturing Institutes (NNMI) to commercialize Wide Band Gap (WBG) power devices. One of the primary goals of the Institute is to achieve significant reductions in the cost of manufacturing WBG devices and achieve price parity with Si IGBTs in the 600 – 1700 V range within 5 years of its inception and fall below today's Si prices in 5-8 years. SiC is considered a post-silicon device for power electronics applications because its superior material properties guarantee low power losses, higher efficiency, and smaller system volume and weight. Since the advent of the first SiC SBD in the 1990's, numerous research groups devoted efforts to commercialize SiC devices, such as MOSFETs, JFETs, BJTs, and thyristors. However, it is believed that massive adoption of SiC power devices will not take place until there are substantial improvements in two major barriers: reliability and price.

The most effective way of achieving price parity to Silicon counterparts is to reduce the material cost that contributes to about 50% of the overall SiC chip cost. Development of large diameter substrates to enhance yield are being pursued by wafer and chip manufacturers. On top of these efforts, device innovation not only reduces chip size, but also directly reduces materials cost reduction. However, there is a lack of quantitative analysis to suggest direction regarding improvement and consequent cost projections.

In this research, methodologies to reduce the chip size of SiC MOSFETs are discussed based on an analytical-empirical model by examining temperature coefficient, junction temperature, on-state resistance, thermal resistance of the package, and edge termination techniques (Fig. 1). In the analysis of chip size, reliability is also taken into consideration because these two factors are mutually related in some aspects. Analyses based on the developed model, lead to following conclusions – even 5 times higher channel mobility of the planar SiC MOSFET can only save 13% of the active area because the temperature coefficient is also increased close to that of SiC bulk resistor; the development of packaging technology to lower the thermal resistance becomes an effective way of reducing the size of the chip; edge termination and periphery area must be reduced to achieve chip-scale reduction in size. This analysis justifies the advanced packaging technologies, such as double-sided cooling, and flip-chip technique.

Finally, the cost analysis based on the proposed model clearly illustrates how the price parity to the Silicon IGBTs can be achieved. Other than the device innovation, from an exemplary cost

analysis, it is found that wafer price, process yield, and wafer size also play significant roles in reducing the chip price (see Fig. 2, and Table 1). Improvement in each parameters discussed in this research should be pursued in parallel to lead to price-parity to silicon devices.
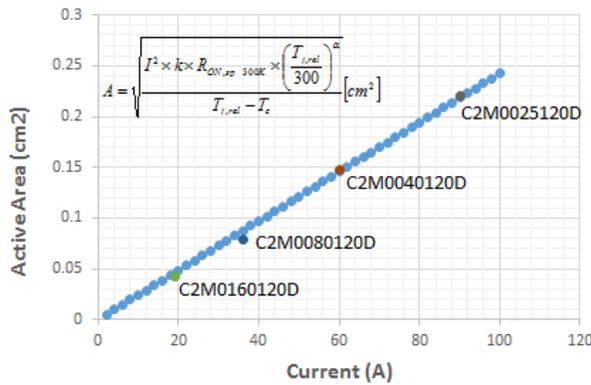

Fig. 1: Active area to target specific currents based on the proposed model (inset). Commercial 1200V SiC MOSFET information are also plotted, and well matched with the model.
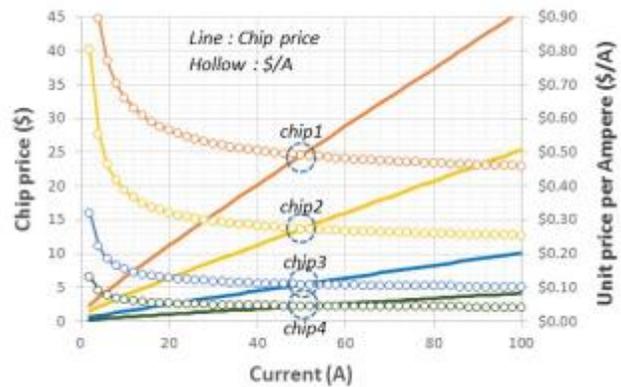

Fig. 2: 1200V SiC MOSFET price projection. Conditions in Table 1 were used in this analysis.

Table 1: Conditions for the exemplary study on the chip price (chip price of 1200V IGBT ~ 0.10 $/A)

	Rth, k (K/W)	Ron,sp (mohm-cm^2)	Tj,max (°C)	Edge Term. (um)	Wafer Price ($)	Yield	Wafer Size (inch)	Wafer Area (cm^2)	$/A (at 50A)
Chip1	0.068	6	150	180	1,500	0.6	4	63.62	*0.491*
Chip2	**0.048**	**3**	**200**	**126**	1,500	0.6	4	63.62	*0.274*
Chip3	0.048	3	200	126	**850**	**0.85**	4	63.62	*0.11*
Chip4	0.048	3	200	126	850	0.85	**6**	**153.93**	*0.045*

TOPIC 2: Area-Efficient Bevel-Edge Termination Techniques for SiC High-Voltage Devices [3]

In recent years, significant improvements in performance have been achieved in SiC devices, such as MOSFETs, BJTs, JFETs, IGBTs, GTOs, JBS, and PiN Diodes. In these high voltage SiC vertical devices, one of the major design concerns is the edge termination. Floating Field Rings (FFRs), or Junction Termination Extension (JTE) -based structures are commonly used edge termination approaches. However, those conventional edge termination techniques consume a significant amount of area on the chip. As a rule of thumb, the edge termination width has dimensions equal to ~5 times the drift region thickness. To reduce the chip size, and thus the cost of the SiC chip, area efficient edge termination techniques are an imperative.

Orthogonal positive bevel edge termination technique has been proposed to produce symmetric blocking structures in SiC. It has been successfully demonstrated that a chip-scale bevel edge termination becomes feasible by using a V-shaped dicing blade as shown in Fig. 3. This technique was successfully demonstrated to achieve high blocking voltage at the substrate-drift layer junction. The bevel edge termination can also be applied to support high voltage at the top PN junctions.

In this study, various innovative edge termination structures using the bevel technique, such as Bevel Junction Termination Extension (Bevel-JTE), Resistive Bevel Termination (RBT), Bevel Assisted JTE (BA-JTE), Positive Bevel Termination (PBT) were investigated. A cross-sectional

view of the Bevel-JTE is shown in Fig. 4 as an example. Device simulation shows a uniform distribution of potential within the Bevel-JTE structure (Fig. 5). The aforementioned non-planar, 3D edge termination techniques significantly reduce the chip size because they require only 1X of the epi-layer in width on the SiC surface.

In general, bevel edge terminations have very low leakage current because the high hardness of SiC smooths the surface morphology when rubbed by the dicing blade (see the I-V curve in Fig. 6). Any residual damage can be then removed by RIE. It should be noted that the Bevel-JTE structure does not even require a photolithography step; CVD oxide, or other properly chosen materials, can be deposited before the dicing step. They can serve as a masking layer for the SiC surface etch treatment process and the JTE ion implantation step. After the bevel groove is inscribed on the wafer, a spray coater can substitute the spin coater for subsequent photolithography processes. Groove filling using a proper dielectric material, followed by a planarization process, can also be a good alternative. Passivation of the bevel surface, and the effect of possible inclusion of negative or positive charges should be further studied.

Since the bevel edge termination is fabricated with a dicing blade, it can be applied to any vertical device in SiC that has a drift layer of different thickness by adjusting the dicing depth. In fact, it is more attractive to use the Bevel-JTE structure for higher voltage devices because a significantly larger area of the wafer is occupied by edge termination structures using conventional approaches. Using the bevel edge termination discussed in this research, significant area can be saved, which in turn contributes to chip cost reduction.
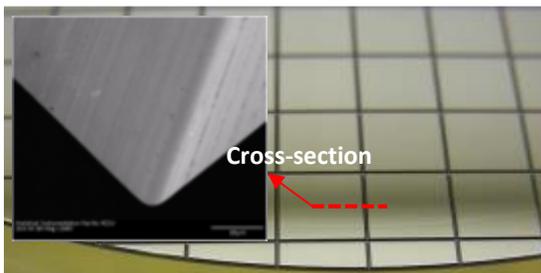
Fig. 3: Wafer image after bevel dicing. Scanning Electron Microscope (SEM) image of bevel surface with 45 degree blade is also shown.
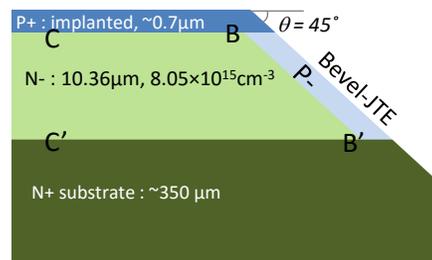
Fig. 4: Cross-sectional view of Bevel-JTE. JTE width for the conventional single-zone JTE is 50µm, while that of Bevel-JTE is about 15µm.
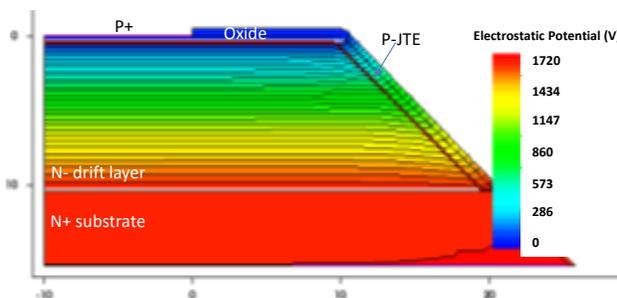
Fig. 5. Potential contour of Bevel-JTE at 1720V. JTE dose in this simulation is $1 \times 10^{13} cm^{-2}$.
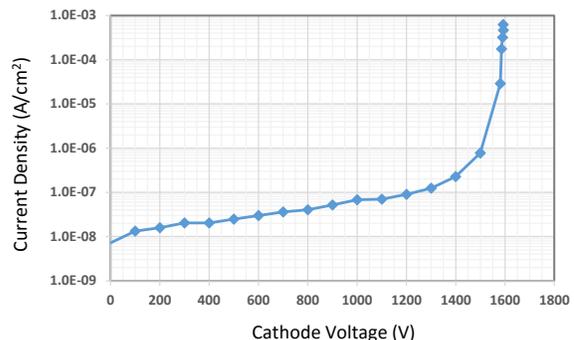
Fig. 6. Typical reverse characteristics of fabricated PiN diodes with Bevel-JTE measured after N_2O RTA process. Implanted JTE dose is $1 \times 10^{13} cm^{-2}$.

TOPIC 3: Development of 1.2kV rated SiC MOSFETs with accumulation mode channel and inversion mode channel [4, 5]

In the past decade, there has been tremendous progress in the electrical performances of 4H-SiC power MOSFETs resulting in their commercialization. However, detailed information on the design of the channel to achieve a reasonable threshold voltage and field effect mobility is lacking in previous literature. Experimental results obtained on both accumulation mode channel design (AccuFETs) and inversion mode channel design (InvFETs) are compared in this research.

Fig. 7 shows cross-sectional diagrams of the 1.2kV SiC vertical power MOSFET and the lateral test structure used to extract the channel mobility. Doping profiles near the SiC surface were optimized by 2-D device simulations in order to accomplish reasonable threshold voltage with high channel mobility. The proposed MOSFETs were fabricated in a 6-inch wafer foundry company, XFAB, TX, U.S.A. Total 9-mask was used for fabrication of the AccuFETs and InvFETs. Fig. 8 shows on-wafer output characteristics of a typical AccuFET and InvFET. Specific on-resistances at drain current of 1A are 4.95 mΩ·cm^2, and 7.75 mΩ·cm^2, for the AccuFET, and InvFET, respectively, at a gate bias of 25V. The average threshold voltages out of 50 AccuFETs, and InvFETs at Id of 1mA are 2.33V, and 4.27V, respectively. Threshold voltages of both structures show tight distributions across the 6-inch wafer (see Fig. 9).
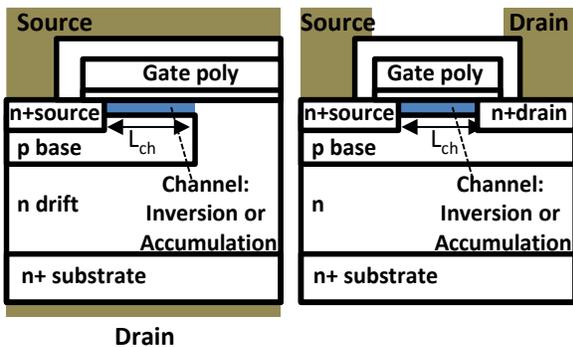
Fig. 7: Cross-sectional views of fabricated SiC Inversion mode and Accumulation mode MOSFETs (Lch=0.5μm), and lateral MOSFET (Lch=200μm)
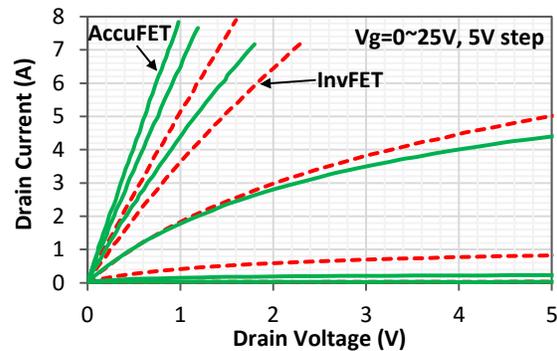
Fig. 8: Typical output characteristics of fabricated SiC AccuFETs and InvFETs. Active area: 4.5 mm^2, measured at room temperature.
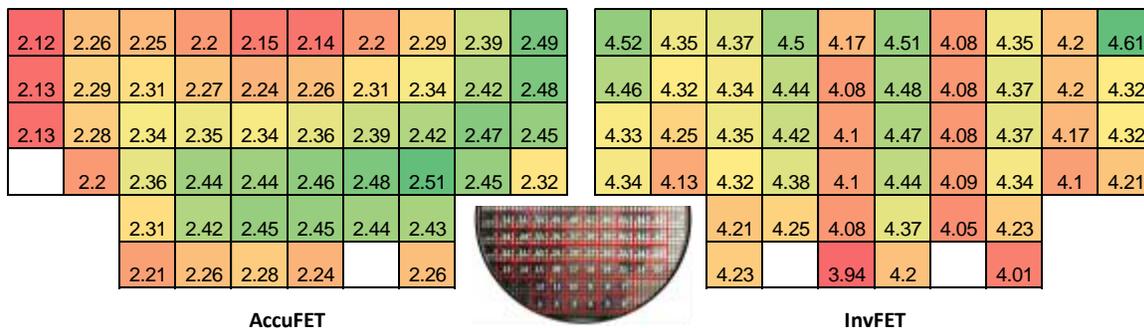
Fig. 9. Distribution of threshold voltages of SiC AccuFETs and InvFETs fabricated on 6-inch SiC wafers. A half-cut picture of a fully processed 6-inch wafer is also shown in the middle. Threshold voltages of AccuFETs show radial pattern across the wafer while those of InvFETs show random distribution.

Field effect channel mobilities were calculated from transconductances measured on lateral MOSFETs with channel length of 200 µm. Fig. 10 shows a good correlation between the accumulation channel mobility and the inversion channel mobility, which may be attributed to common process variations such as the gate oxide thickness and the subsequent annealing. A clear correlation between the threshold voltage and the channel mobility was observed for both AccuFETs and InvFETs as shown in Fig. 11. This correlation is informative to establish the gate oxidation and post oxidation anneal (POA) process. Threshold voltages and channel mobilities at high temperatures were also compared (not shown in this report). It was also proven that no significant deterioration was produced in blocking characteristics by both channel designs.

In summary, the 1.2kV AccuFET structure provides lower on-resistance, and higher transconductance due to higher channel mobility compared with the 1.2kV InvFET. The threshold voltage of the AccuFET structure is about 2V lower than that of the InvFET structure, but still in the acceptable range.
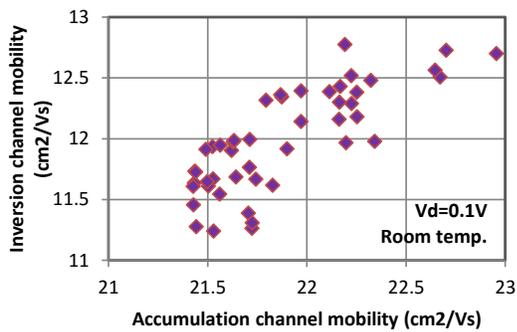
Fig. 10: Field effect channel mobilities extracted from Id-Vg of 52- lateral MOSFETs. L_{ch}=200 µm, Channel width=200 µm. V_d=0.1V, V_g=20V.
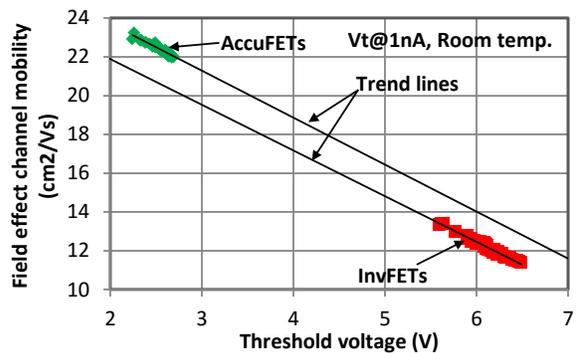
Fig. 11: Trade-off between channel mobility and threshold voltages. All data were measured from lateral MOSFETs. Channel designs and gate oxidation processes determine this trade-off.

TOPIC 4: Monolithically Integrated 4H-SiC MOSFET and JBS Diode (JBSFET) using a Single Ohmic/Schottky Process Scheme [6, 7]

Bipolar operation of the inherent body-diode in a Silicon Carbide (SiC) MOSFET structure is undesirable for reliable device operations and reduced conduction loss. A Schottky contact based unipolar-type diode can be externally connected in parallel to a MOSFET as a separate chip in order to accommodate current in the opposite direction. In this case, the body-diode formed by the p-well and n-drift junction in the MOSFET structure will not turn-on. When a unipolar mode diode is integrated in a MOSFET structure on a single chip, it is beneficial because both MOSFET and diode not only share the forward conducting layer but they also share the edge termination region such that a significant reduction in SiC wafer area can be expected. In addition, this approach will reduce the number of packages in half bringing down the cost of implementing this technology in power converters. It will also improve efficiency and increase switching frequency by eliminating the parasitic inductance between separately packaged devices. Various approaches for a MOSFET and

- The inherent pn body diode works as a freewheeling diode; No need of an external diode.
- The pn body diode conduction results in degradations such as a diode forward drop drift, and MOSFET Ron increase.

- A SiC MOSFET is paired with an external unipolar SiC diode.
- Larger number of packages, larger converter size, and larger parasitic inductances.

- SiC MOSFET with integrated unipolar internal inverse MOS-Channel Diode (Panasonic).
- Reverse current flows through the MOS channel with zero bias of the gate; doping, and thickness of the channel should be carefully chosen.

- Monolithic integration of Schottky or JBS diode in a SiC MOSFET structure (JBSFET).
- SiC MOSFET and JBS diode share the edge termination structure as well as drift layer; Smaller size of package, lower inductance.

Fig. 12: Various approaches to accomplish SiC MOSFET and diode pair in a power converter application.

diode pair are summarized in Fig. 12. Panasonic proposed a MOSFET structure integrated with unipolar internal MOS-channel diode. However, since its diode structure is utilizing the MOSFET channel, and a diode requires a certain knee voltage, it is difficult to attain balanced current handling capabilities from both MOSFET and diode at the same forward voltage drops. In addition, n-epitaxial channel needs to be engineered to ensure diode current at reasonable voltage drop, which may bring issues in process latitude, and other reliability concerns in the MOSFET operation. Hestia Power Incorporation and Mitsubishi also demonstrated a MOSFET with embedded diode. In their approaches, Schottky region was formed by a separate metal process.

In this research, a simple method to accomplish a unipolar antiparallel Junction Barrier Schottky (JBS) diode functionality within the SiC MOSFET structure was proposed and experimentally verified for the first time. A simple fabrication scheme has been developed for the proposed JBSFET in order to avoid adding any processing steps to the conventional MOSFET fabrication flow.

Fig. 13(a) shows the layout of the proposed SiC JBSFET. The pure JBS diode area is surrounded by MOSFET cells. It is convenient to place the MOSFET outside because the gate pad does not interrupt the big source pad, which makes the wire bonding easier, and the wire to the gate pad shorter. Area for each MOSFET and JBS diode can be determined through 2-D

device simulations to target a specific current. A cross-section of the proposed SiC JBSFET is shown in Fig. 13(b). It is important to note that a single metal, single thermal treatment process was used to simultaneously form ohmic contacts on n+, p+ implanted regions, and Schottky contact on n- 4H-SiC epi-layer. Nickel (Ni) is the most commonly used metal for the ohmic contact formation on n+ region on SiC with a RTA process at higher than 950°C. Ni is also able to form an ohmic contact on p+ implanted region at the same time. However, there are no detailed reports on the formation of n- Schottky contacts simultaneously with n+ and p+ ohmic contacts. For the purpose of this work, Ni is required to remain a Schottky contact on n- epi-layer after the RTA process. Therefore, careful investigation to optimize the RTA condition was required. It was found that Ni can simultaneously form ohmic contacts on n+ and p+ implanted regions while it remains a Schottky contact on the n-epitaxial drift layer when it is annealed at moderate temperature (900°C for 2 min). Fig. 14(a) shows typical output characteristics of the fabricated JBSFET and MOSFET. As expected, the MOSFET has a lower on-resistance than the JBSFET in the forward conduction mode (first quadrant) due to the area consumed by the JBS diode. At the same active area (4.5 mm^2), specific on-resistances at drain current of 1A are 7.25 mohm·cm^2 and 12.5 mohm·cm^2 for the MOSFET and the JBSFET, respectively. However, in the third quadrant, the JBSFET provides a very low forward drop due to the conduction of the JBS diode as shown in Fig. 14(b). In contrast to the MOSFET, the JBSFET shows exactly same current-voltage characteristics regardless of the gate biases. It should be noted that it is flexible to achieve a desired current in each first and third quadrant from the JBSFET by allocating appropriate area in its layout design.


(a)   (b)
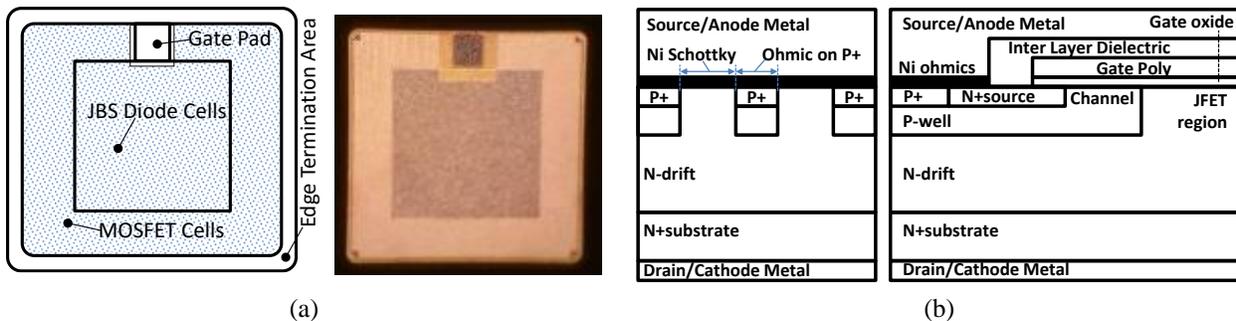
Fig. 13: (a) Schematic diagram of JBSFET layout and the chip image and (b) Cross-sectional view of JBS diode cell structure (left) and MOSFET cell structure (right). It is important to note that a single process, multi-purpose Ni contacts on 4H-SiC was used. The Schottky width is 4 µm and the cell pitch for the MOSFET is 11 µm with the channel length of 0.8 µm.

(a)   (b)
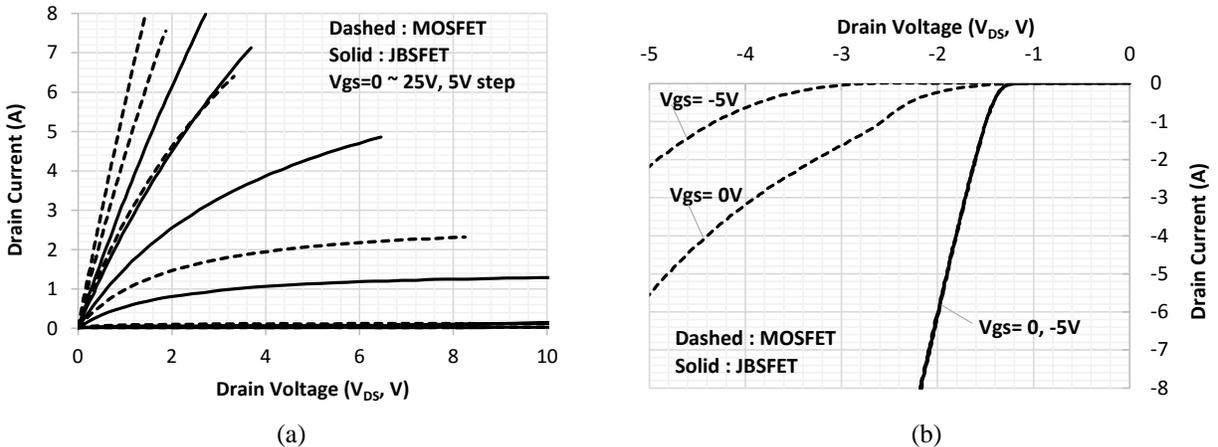
Fig. 14. Comparison of (a) the first and (b) third quadrant behaviors of the fabricated JBSFET and MOSFET. The JBSFET was annealed at 900°C for 2 minutes while the MOSFET was annealed at 950°C for 2 minutes. Both JBSFET and MOSFET have the same active area: 4.5 mm^2. But, in the JBSFET layout, only 45 % of the active area was allocated for the MOSFET cells. Threshold voltages for both devices are the same: 2.7V at I_d=1 mA. All data were measured on wafer at room temperature.

TOPIC 5: Edge termination techniques for high voltage devices on SiC [8, 9]

Conventional edge termination techniques for SiC devices include floating field rings (FFRs), junction termination extension (JTE), and modified JTE structures. Among these edge termination structures, FFRs usually require a narrow definition of the space between rings near the main p+/n junction, and tight control of defects in order to achieve the designed breakdown voltage. It is widely known that a conventional single zone JTE (SZ-JTE) is sensitive to the impurity dose resulting in a sharp peak in breakdown voltage over the JTE implant dose. The optimum JTE dose for the SZ-JTE is about 1×10^{13} cm^{-2} based on the Gauss law. To overcome this shortcoming, multiple floating zone JTE (MFZ-JTE) and space modulated JTE (SM-JTE) were proposed, which experimentally verified that high breakdown voltage can be achieved at higher dose in JTE region. Ring assisted JTE (RA-JTE) was proposed to provide high breakdown voltage with a lower JTE dose than the one optimized for the SZ-JTE.

In this research, a Hybrid-JTE that combines MFZ-JTE and RA-JTE is proposed to achieve a near ideal breakdown voltage over a wide range of JTE dose for the first time. A conventional FFR structure that consumes the same area was designed and fabricated at the same time for a comparison purpose.

Fig. 15(a) shows the proposed Hybrid-JTE structure that simply combines a RA-JTE and a MFZ-JTE structure. 40μm thick-, 2×10^{15}cm^{-3} doped drift layer was chosen to attain 5500V from a parallel plane p+n diode. 35-FFRs was also designed and optimized based on extensive 2-D simulations (Fig. 15(b)). Total width for both Hybrid-JTE and FFRs is 180 μm. Each RA- and MFZ-JTE is designed exclusively and then combined to create the proposed Hybrid-JTE structure.

Fig. 16 shows measured reverse blocking characteristics of the fabricated PiN diodes with the proposed Hybrid-JTE structures and FFRs. The maximum breakdown voltage achieved by using the Hybrid-JTE was 5450V at anode current of 100 μA, which is 99% of the ideal value for a 1-D structure calculated using Konstantinov's form for the critical electric field for our structure. From most of dies, the leakage current is maintained very low up to 4000V. In contrast, the maximum breakdown voltage from the PiN diode with FFRs was 4160V. Furthermore, a

significant increase in leakage current is observed at relatively low voltage at ~2000V. Overall, it was experimentally demonstrated that the Hybrid-JTE provides a nearly ideal breakdown voltage with tight distribution across the wafer. In addition, wider range of JTE implant doses were allowed for achieving high breakdown voltages using the Hybrid-JTE.

(a)   (b)
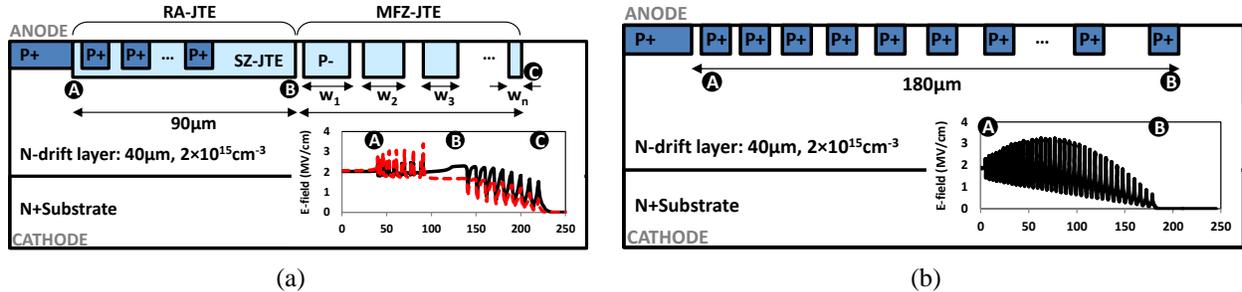
Fig. 15: (a) Cross-sectional view of the proposed Hybrid-JTE structure. 6-rings are placed in the consecutive SZ-JTE to relieve electric field at location 'A'. Exclusively optimized MFZ-JTE structure is placed next to the RA-JTE relieving electric field at location 'B'. Rings for RA-JTE are formed by the P+ main junction implant. Discrete charge zones for MFZ-JTE and SZ-JTE region are formed by single implant process, (b) Cross-sectional view of floating field rings (FFRs) termination structure. 3μm wide 35-ring consumes 180μm in width. Simulated electric fields at the breakdown condition are shown in the insets; for the Hybrid-JTE, the dashed line indicates a low dose (9×10^{12} cm^{-2}) and the solid line shows a high dose case (1.25×10^{13} cm^{-2}).

(a)   (b)
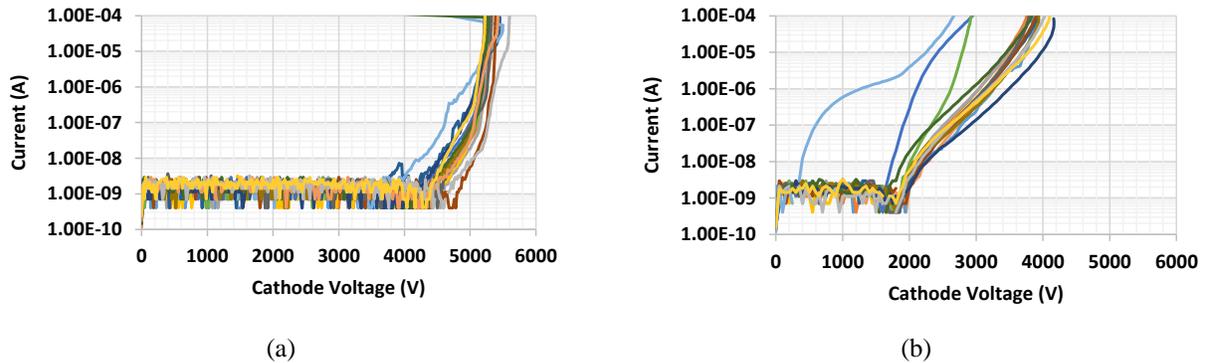
Fig. 16: Blocking behaviors of randomly selected 16-PiN diodes with (a) Hybrid-JTE, dose=1.8×10^{13} cm^{-2}, (b) 35-FFR.

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MultiBeam Scanning Electron Microscopy for Nanoscale Manufacturing Metrology
(Thiel Research Group)

Scope: Assess the viability for multibeam/multicolumn SEM approaches to address advanced nanoscale manufacturing metrology requirements

Goals:
1. **Identify performance requirements for a range of application spaces**
2. **Develop appropriate testing methodologies and test structures**
3. **Develop simulation processes for generating large image data sets containing statistical process variations, including pattern defects and critical dimension variations**
4. **Develop algorithms for assessing and predicting tool performance variations**
5. **Develop algorithms for determining detection sensitivity limits to process variations based on tool performance and operating parameters**

2016 Accomplishments

TOPIC 1

An experimental means for determining the Contrast Transfer Functions from an array of electron beams has been developed. The process consists of first obtaining images from a specimen exhibiting a known, and preferably flat, distribution of spatial frequencies. The second step comprises obtaining the radially integrated Fourier transform of the image, and removing the specimen information, leaving the true fidelity with which the system responds as a function of spatial frequency.

A specimen meeting these requirements was produced by creating SiO_2 dots on a silicon wafer using electron-beam lithography with a 12 nm design rule. Because the random dot array (RDA) was produced using a Graphic Database System (gds) file, the location of each of dot is known, and therefore the distribution of spatial frequencies can be determined exactly. The next stage of the effort was to determine the exact shape of the dots using atomic force microscopy and transmission electron microscopy of cross sections. The secondary electron emission behavior of the dots can be simulated (see Topic 2 below), to produce the shape function of the dot features. The shape function is then convolved with the known spatial distribution to produce the complete Fourier signature of the specimen. When the transform of the real image is divided by the specimen signature, the actual contrast transfer function is revealed.

TOPIC 2

A multiscale modeling approach was developed to generate virtual image data sets of patterned wafers containing randomly generated processing defects. Defects could include linewidth variations or a range of pattern defects, including gaps, bridges and particles. A "tiling" approach was used where the ideal secondary electron emission profiles of an ideal structure was generated (e.g., a single fin within a finFET array). A mosaic image is constructed from the ideal tile, modulating the individual pixel intensities with stochastic variations due to background, shot noise, and effects of electron-optical aberrations associated with realistic operating conditions. Further, defect tiles representing process variations or patterning defects can be randomly inserted to mimic a realistic data set. This virtual dataset is then assessed by an additional suite of algorithms developed to represent a particular type of metrology, such as defect inspection or CD measurements.

Using these simulations, it is possible to estimate the performance of a virtual tool against requirement specifications, and assess the impact of material set, device architecture, design rules, and operating conditions. Conversely, the impact of throughput requirements on defect or CD sensitivity can be assessed for a given application.
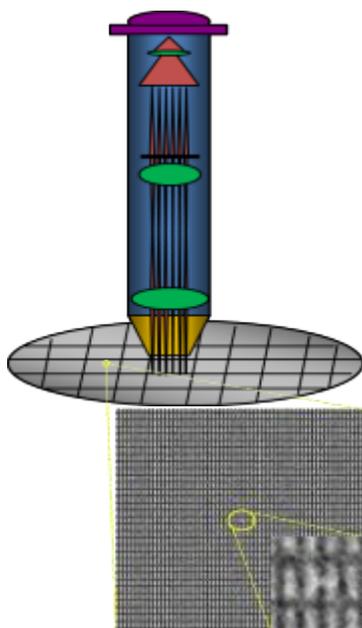
Figure 1: Schematic of a multibeam mosaic image.
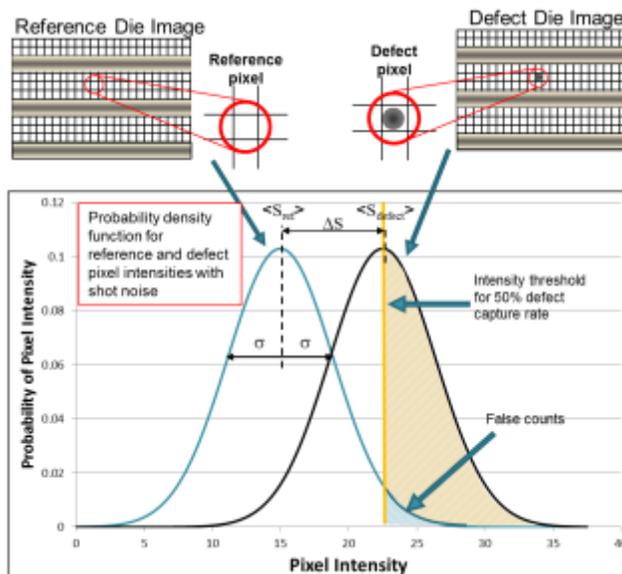
Figure 2: Probability distributions for ideal and defective pixel intensities.
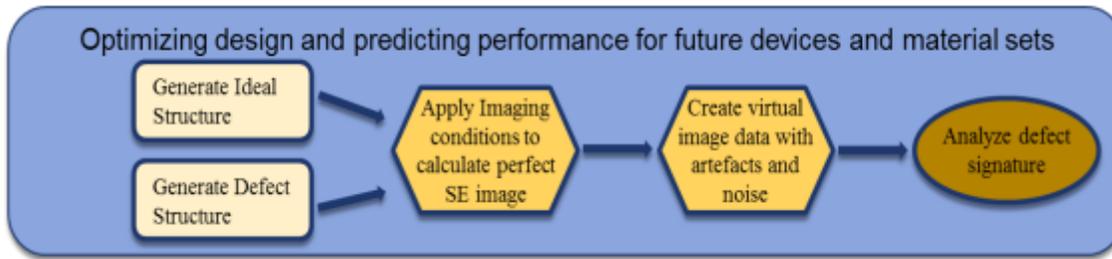
Figure 3: Flowchart for virtual image data generation.

Related Publications

Image Simulation and Analysis to Predict the Sensitivity Performance of a Multi-Electron Beam Wafer Defect Inspection Tool, Maseeh Mukhtar, Kathy Quoi, Benjamin D Bunday, Matt Malloy and Brad Thiel, Microscopy and Microanalysis **22** (Suppl. 3) 620-621 (2016).*

   *Microscopy & Microanalysis 2016 Student Poster award

Patterned Wafer Inspection with Multi-beam SEM Technology
Brad Thiel, Maseeh Mukhtar, Kathy Quoi, Benjamin D. Bunday and Matt Malloy, Microscopy and Microanalysis **22** (Suppl. 3) 586-587 (2016).

Measuring multielectron beam imaging fid elity with a signal-to-noise ratio analysis
Maseeh Mukhtar ; Benjamin D. Bunday ; Kathy Quoi ; Matt Malloy ; Brad Thiel
Journal of Micro/Nanolithography, MEMS, and MOEMS | Volume 15 034004 (2016).

Nano-Device Research
(Bin Yu Group)

Scope:
Prof. Yu's lab is conducting research in the following areas:
- **(i)   Emerging memory devices**
- **(ii)   Post-Cu interconnects**
- **(iii) Nano-sensors**
- **(iv) Nanomaterials synthesis & characterization**

Goals: To advance the arts of nanodevice (physics, engineering, and technology) based on a range of functional 1D/2D/3D nanomaterials.

2016 Accomplishments

TOPIC 1: Resistive Switching on 2D Nanosheets

Two-dimensional (2D) van der Waals crystals are viable material platforms for future nanoelectronic devices, potentially exhibiting low-power operation, mechanical flexibility, transparency, and low fabrication cost. As one of the key elements in electronics, it would be interesting to demonstrate non-volatile memory (NVM) comprised exclusively of a single 2D nanosheet. We recently observed resistive switching behavior in 2D layered Sb_2Te_3 nanosheets. Due to crystalline-amorphous phase transitions under the melt-quench-recrystallization mechanism, hysteretic behavior were observed and the on/off ratio in electrical resistance was more than two orders of magnitude. The memory behavior was shown to be non-volatile. We also observed that the programming energy required to amorphize Sb_2Te_3 nanosheets is decreased exponentially with layer thickness, indicating possibly ultra-low power consumption for scaled phase-change nanosheet down to the physical thickness limit (In the Sb_2Te_3 case, 1 nm for 1 quintuple layer).

The experimental demonstration of resistive switching phenomenon in two-dimensional phase-change nanostructures opens up the possibility of developing high-capacity and low-power non-volatile memory and programmable logic. Ultra-scaled two-dimensional chalcogenide phase-change devices could lead to the conceptual synaptronic computing, which may meet or even exceed the energy efficiency of neuro-biological architectures.
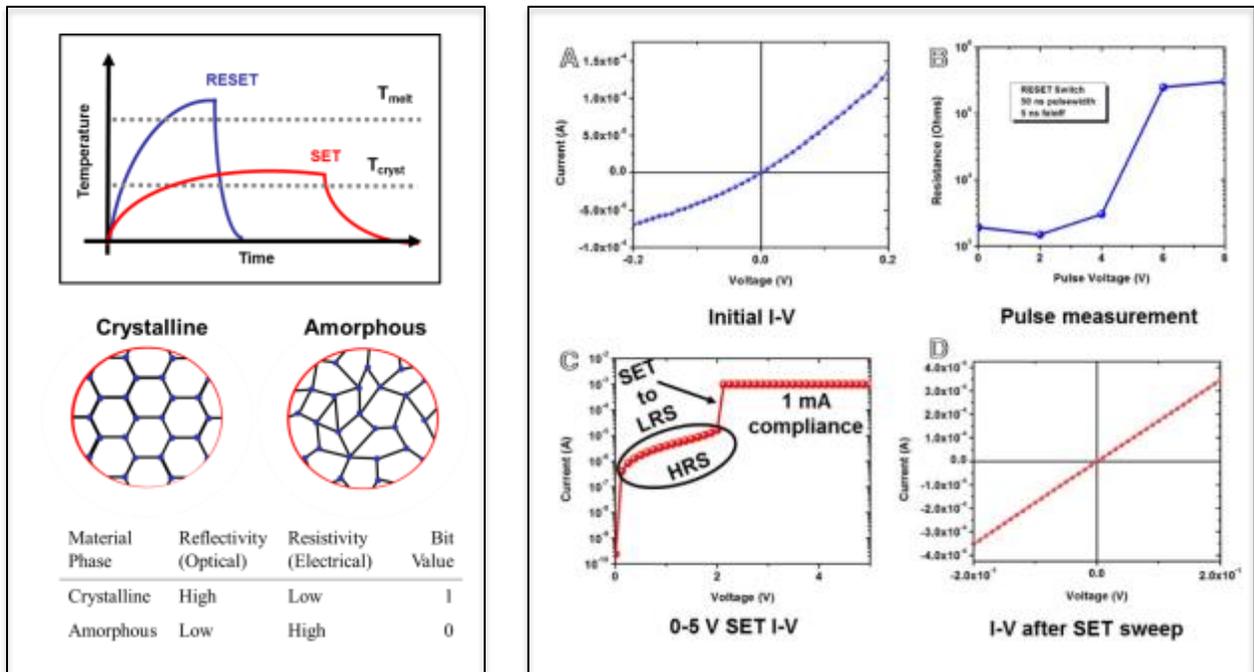
Figure 1: Resistive switching demonstrated on 2D Nanosheet. (Left) Schematic diagrams showing the operating principal of phase-change material under the melt-quench mechanism. **(Right)** Device behaviors: (A) Initial I-V data shows the nanosheet resistance in its initial low-resistance-state (LRS). (B) Device is subjected to a voltage pulsed with 50 ns width and 5 ns edge times. A switch to the high-resistance-state (HRS) is observed for pulse amplitudes greater than 6 V. (C) A high voltage I-V is performed to RESET the device to LRS, in line with the early experiments done by Waterman, *et al*. (D) A low voltage I-V sweep confirms the return to the original crystalline phase. The small decrease in resistance and increase in linearity of the I-V sweep over that in (A) can be attributed to contact annealing during pulsing.

TOPIC 2: Graphene-Based Interconnects

Low current capacity, high power dissipation, and increased RC-delay are the major challenges toward achieving ultra-scaled, high-speed interconnects for integrated circuits, and are the main factors driving research in the area. The performance limitation in Cu wires is attributed to carrier scattering at material interfaces and grain boundaries, as well as electromigration and heat-induced failure at scaled dimensions. Recently, graphene has emerged as a front runner for interconnect design in the post-Cu era, due to its excellent material properties, including high breakdown current and robustness to electromigration. Although monolayer graphene shows current densities over 10^8 A/cm^2, ~100 times higher than Cu, its atomically-thin nature limits the overall current capacity.

Multi-channel graphene stack is one of the promising directions to implement carbon-based interconnects. However, interlayer carrier scattering hampers the conduction in two-dimensional layered stacks. In this work, we have demonstrated dual-layer graphene (DLG) structure with h-BN (2D insulator) as the intercalating layer. The DLG employs graphene grown by chemical-vapor-deposition (CVD) with h-BN serving as a barrier

preventing interlayer scattering. Raman spectrum shows signature peaks with enhanced sharpness, as compared with bilayer graphene. The density-functional-theory (DFT) simulation shows degenerate energy bands in the *E-k* dispersion. The decoupling of graphene monolayers is further confirmed by electrical measurements. The conduction in DLG structures is compared with monolayer graphene and randomly stacked bilayer graphene. Extenuated carrier scattering is observed in DLG wire, showing higher current-carrying capacity and maximum power density. In addition, the DLG is shown to be robust under voltage stressing at an elevated temperature (150°C) with the mean-time-to-failure (MTTF) ~75 times higher than that of stacked bilayer graphene. The demonstrated electrical characteristics in the DLG heterostructure suggests a pathway to preserve the carrier transport of graphene monolayer in a multi-channel configuration, leading to potential implementation of highly conductive systems.
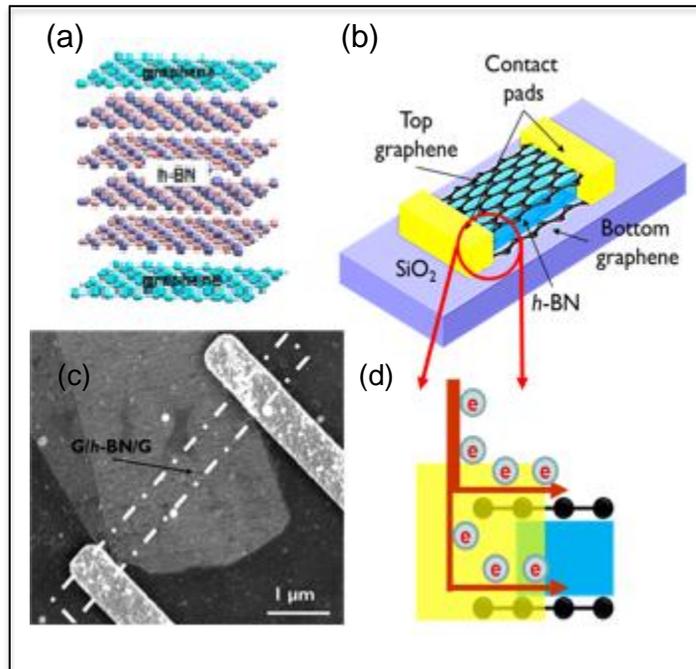
Figure 2: Carbon-based Interconnects. (a) Atomic-lattice schematic of a double-layered graphene (DLG) heterostructure separated by an interposing h-BN multilayer; (b) SEM image showing the heterostructure with two probing contacts. Here, the dash-dotted lines show the edges of plasma-etched graphene ribbon for eye-guiding purpose. (c) Schematic tilted-view of the DLG structure. (d) Zoomed-in view showing the detail of graphene-metal contact.

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Michael Carpenter

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Gregory Denbeaux

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10. Narasimhan, Amrit; Grzeskowiak, Steven; Ackerman, Christian; Flynn, Tracy; Denbeaux, Greg; Brainard, Robert L; "Mechanisms of EUV exposure: electrons and holes", Extreme Ultraviolet (EUV) Lithography VIII, 10143, 101430W, 2017

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1. Amrit Narasimhan, Steven Grzeskowiak, Robert Brainard, Greg Denbeaux, "EUV Testing:Acid quantum yield and optical density" Dow Chemical (October 2016),
2. Steven Grzeskowiak, Amrit Narasimhan, Christian Ackerman, Jake Kaminsky, Daniel Freedman, Robert Brainard, Greg Denbeaux, "The role of secondary electrons in EUV resist exposure mechanisms", Hiroshima Japan IEUVI Resist TWG meeting (October 2016)
3. Steven Grzeskowiak, Amrit Narasimhan, Michael Murphy, Jodi Hotalen, Christian Ackerman, Jake Kaminsky, Lee Napolitano, Daniel Freedman, Robert Brainard, Greg Denbaeux, "Comparison of EUV and electron reactivity for metal oxalate photoresists", San Jose, CA, IEUVI Resist TWG meeting (February 2017)
4. Steven Grzeskowiak, Amrit Narasimhan, Michael Murphy, Lee Napolitano, Daniel Freedman, Robert Brainard, Greg Denbeaux, "Reactivity of metal oxalate EUV resists as a function of the central metal", Berkeley CA, EUVL Workshop (June 2017), **Invited**
5. San Jose, CA, SPIE Advanced lithography conference (February 2017), multiple presentations by students or other collaborators:

6. Michael Murphy, Robert Brainard, Greg Denbeaux et al., "EUV exposure mechanisms of antimony resists", San Jose, CA, SPIE Advanced lithography conference (February 2017)
7. Steven Grzeskowiak, Robert Brainard, Greg Denbeaux et al., "Reactivity of metal-oxalate EUV resists as a function of the central metal", San Jose, CA, SPIE Advanced lithography conference (February 2017)
8. Yudhishthir Kandel, Robert Brainard, Greg Denbeaux, et al., "Correlation of experimentally measured atomic scale properties of EUV photoresist to modeling performance: an exploration", San Jose, CA, SPIE Advanced lithography conference (February 2017)
9. Amrit Narasimhan, Robert Brainard, Greg Denbeaux, et al., "Mechanisms of EUV exposure: electrons, holes, and molecular interactions", San Jose, CA, SPIE Advanced lithography conference (February 2017)

Technology Disclosure
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Harry Efstathiadis

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Pradeep Haldar

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Ji-Ung Lee

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3. 2nd Annual The Society for Neuroscience Hudson-Berkshire Chapter, "The future of penetrating Neural Probes", The Carey Institute for Global Good in Rensselaerville on **Monday September 19, 2016**.
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Shadi Shahedipour

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Natalya Tokranova

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Bin Yu

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