NPTEL Online Certification Course
<Design of Power Electronics converter>
<Assignment Number 1>: Detailed Solution
Indian Institute of Technology Guwahati

Q1. The first two steps to design a power electronic converter are:

Ans. a,b

Q2. During the analysis of a power electronic converter, which among the following should be studied for designing the converter:

Ans. a,c,d,e,f

Q3. What is the use of finding out the maximum modulation index, for a given modulation strategy, in designing an inverter?

Ans. b,c

Q4. Which of the following modulation strategy will be most suitable for designing a single-phase inverter?

Ans. a

Q5. For a certain application an UPS is designed. It contains an H bridge inverter as one of the main conversion stages inside. To obtain a sinusoidal voltage at the output of UPS, the output of the H bridge is connected to a low pass LC filter. Initially, the power electronic engineer designed the UPS using bipolar PWM. Later the engineer decided to change the modulation strategy to unipolar PWM. Which of the following is/are true?

Ans. d

For Problems 6 to 15, note the following important instructions for entering answer: Enter answers upto two decimal places. For example: 3.00 Apply rounding off. For example: enter 5.375 as 5.38 and 5.374 as 5.37. Solve all problems dependent on answers of previous steps, using values obtained after rounding off upto two decimal places in previous steps. Do not enter the unit. A buck converter needs to be designed with following specifications:

Input voltage V_{in}: 40 V

Output voltage V_o: 30 V

Peak output power P_o: 150 W

Maximum ripple in output voltage: 0.1% of V_o

The buck converter should remain in CCM for the load range of 50 W to 150 W. The maximum ripple allowed in inductor current is limited to 15% of load current Io. A switching frequency of 100 kHz can be used. Calculate the following: The voltage rating of X component should be above .... V.

Q6. X=MOSFET

Ans. 40 V. The maximum voltage across the MOSFET is the supply voltage when it is not conducting.

Q7. X=Diode

Ans. 40 V. The maximum voltage across the diode is the supply voltage when it is not conducting.

Q8. X=Capacitor

Ans. 30 to 30.03 V

$$V_{cpeak} = V_c + \frac{\Delta V_c}{2}$$

Based on the limit on current ripple, the current rating of X component should be above .... A

Q9. X=MOSFET

Ans. 5.35 to 5.40 A

$$I_{Lpeak} = I_L + \frac{\Delta I_L}{2}$$

Q 10. X=Diode

Ans. 5.35 to 5.40 A.

I_{Lpeak} remains same for the Diode as calculated in Q 9.

Q 11. X=Inductor

Ans. 5.35 to 5.40 A.

I_{Lpeak} remains same for the Inductor as calculated in Q 9.

Q 12. . The value of $L_{critical}$ is .... μH.

Ans. 22.45 to 22.51

D=$\frac{V_o}{V_{in}}$

$$I_{OB} = I_{LB} = \frac{P_{OB}}{V_{in}};\ P_{OB}$$

$$L_{Critical} = \frac{(V_{in} - V_o)DT_s}{2I_{LB}}$$ =50 W

Q13. The value of L_{ripple} is .... μ H. (Note: You need to consider the entire load range given for CCM.)

Ans. 299.5 to 300.5

For load range of 50 W to 150 W, we perform calculations at peak power and boundary powers.

$$I_{Opeak} = I_{Lpeak} = \frac{P_{Opeak}}{V_{in}}$$

ΔI_L = 15% of I_L

$$L_{ripple} = \frac{V_{in}(D)(1-D)}{f_s \Delta i_l}$$

Calculate L_{ripple} for peak and boundary Δi_l.

Select the larger inductance value to ensure CCM operation for the entire range.

Q14. Based on the above calculations, which among the following value of L you'll choose for the design.

Ans. c

Q15. Calculate the value of C in .... μF, to satisfy the specified limit on ripple in output voltage.

Ans. 8.90 to 8.95

$$C = \frac{V_{in}D(1-D)}{8Lf_s^2 \Delta V_o}$$

Q16. Based on the above calculations, which among the following value of C you'll choose for the design.

Ans. d