Week: 5

1. Pick Wrong statements

(i) Logical Effort of n-input NAND gate is (n+2)/3
(ii) Parasitic Delay of n-input NAND gate is n
(iii) Parasitic Delay of n-input NOR gate is n
(iv) Logical Effort of Tristate Inverter is 2
(v) Falling Elmore delay of n-input NAND gate is [(n^2+5n)/3].RC
(vi) Parasitic Delay of Tristate Inverter is 2
(vii) Logical Effort of n-input NAND gate is (2n+1)/3
(viii) For a given gate, Liner delay value is always more than or equal to Elmore delay.
(ix) Logical Effort of Select line(S) in 2~input Tristate Multiplexer is 4
(x) Falling Elmore delay of n-input NOR gate is [(n^2+5n)/3].RC
(xi) Logical Effort of n-input NOR gate is (2n+1)/3
(xii) Logical Effort of Data line (D0 or D1) in 2~input Tristate Multiplexer is 2
(xiii) Parasitic Delay of 4~input Tristate Multiplexer is 8
(xiv) Falling Elmore delay of n-input NAND gate is [(n^2+5n)/2].RC
(xv) Logical Effort of n-input NOR gate is (n+2)/3

a) v, vii, viii, x, xv
b) v, vii, viii, ix,
c) i, v, xi, x, xv
d) ii, iii, xiii, vii, xv
e) iv, vi, ix, xiii, xi
f) vi, viii, ix, xii, xv
g) xi, xii, xiii, xiv, xv
h) v, vii, viii, x, xiii

2. In the context of the short-channel model of transistors, what is the logical effort of a 2-input NOR gate?

a) 1.667
b) 1
c) 1.500
d) 1.111
e) 0.667
f) 0.6
g) 0.5
h) 0.9

3. How many unskewed inverters of 2:1 size is required to design a ring oscillator operating at 1.32 GHz for a 65 nm technology? Consider RC = 1 ps.

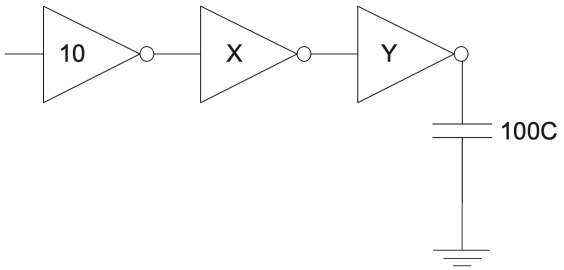
a) 31
b) 32
c) 62

d) 63
e) 292
f) 33
g) 13
h) 132

4. If R=10KΩ, C = 0.1fF is the switching resistance and parasitic capacitance respectively for a unit NMOS transistor, determine the propagation delay of the driving inverter which is sized P:N as 4:2, and connected to 11 inverters in parallel of size P:N as 8:4?

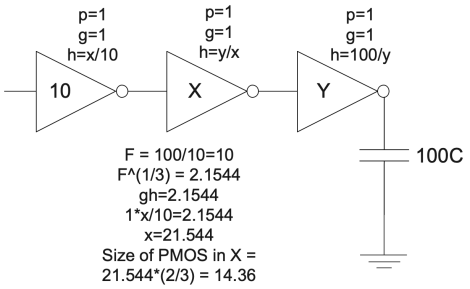
a) 18 ps
b) 12 ps
c) 32 ps
d) 3.13 ns
e) 330 ps
f) 69 ps
g) 310 ps
h) 3.19 ns

5. To achieve optimal delay in the provided circuit, what should be the sizing of the PMOS transistor in Inverter "X"?

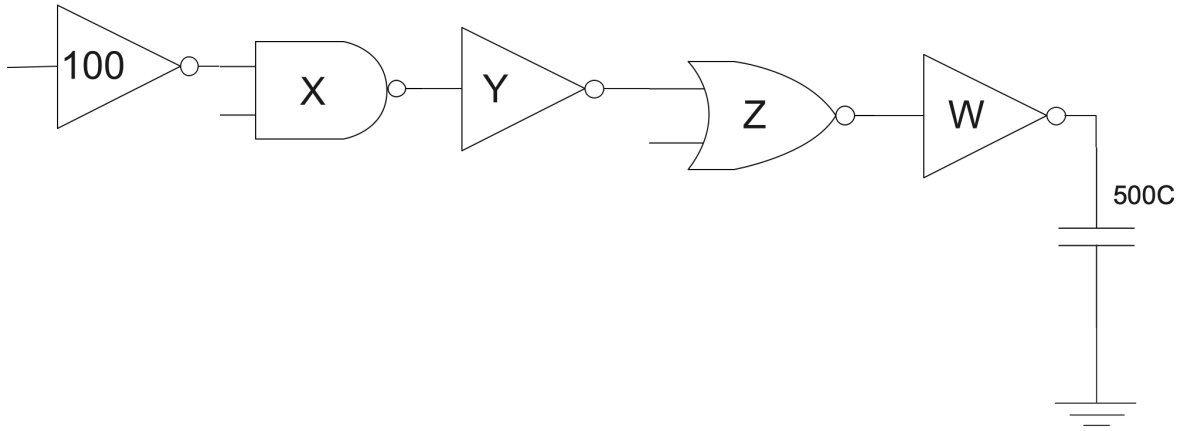


a) 21.15
b) 2.15
c) 1.436
d) 7.18
e) 2
f) 6.667
g) 14.36
h) Impossible to determine.

Solution:

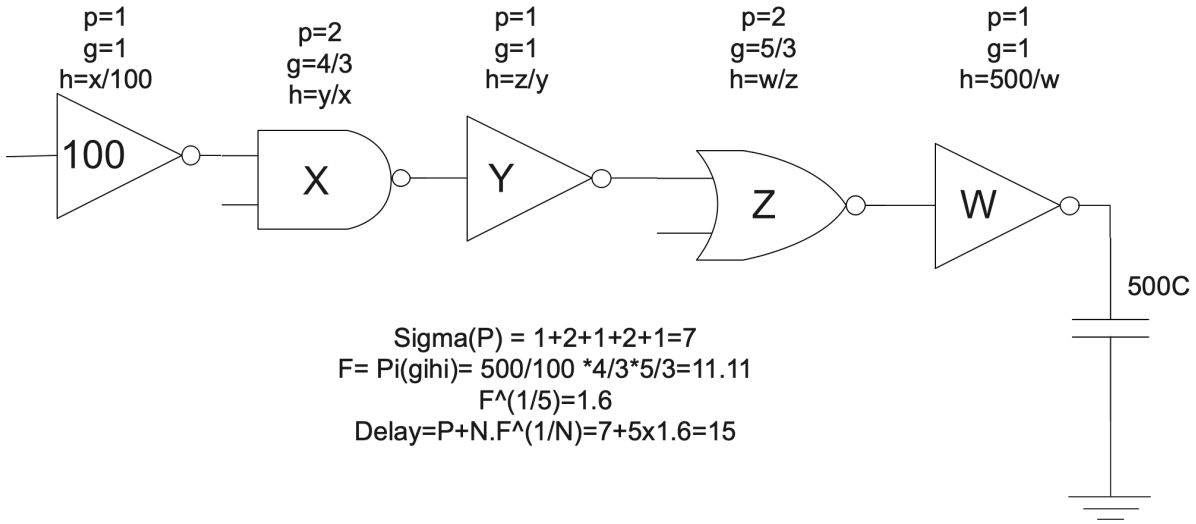


6. Find the optimal normalized delay of circuit.



a) 45
b) 45.5
c) 13.5
d) 15
e) 11.8
f) 12
g) 10
h) 8

Solution:



Sigma(P) = 1+2+1+2+1=7
F= Pi(gihi)= 500/100 *4/3*5/3=11.11
F^(1/5)=1.6
Delay=P+N.F^(1/N)=7+5x1.6=15

7. In the process of optimizing the circuit for the number of stages, the ideal value for F^(1/N) should closely approximate which of the following options?

a) 3.253
b) 32.53
c) 2
d) 2.253
e) 5
f) 1.253
g) 3.591

h) 22.53

8. In a complex digital circuit, the path effort of the critical path is 1927 and for the current design, critical path includes 6 stages. If the designer can adjust the gate sizes in all stages and can add more inverter stages, how many extra inverter stages are required to finetune the delay to a optimal value?

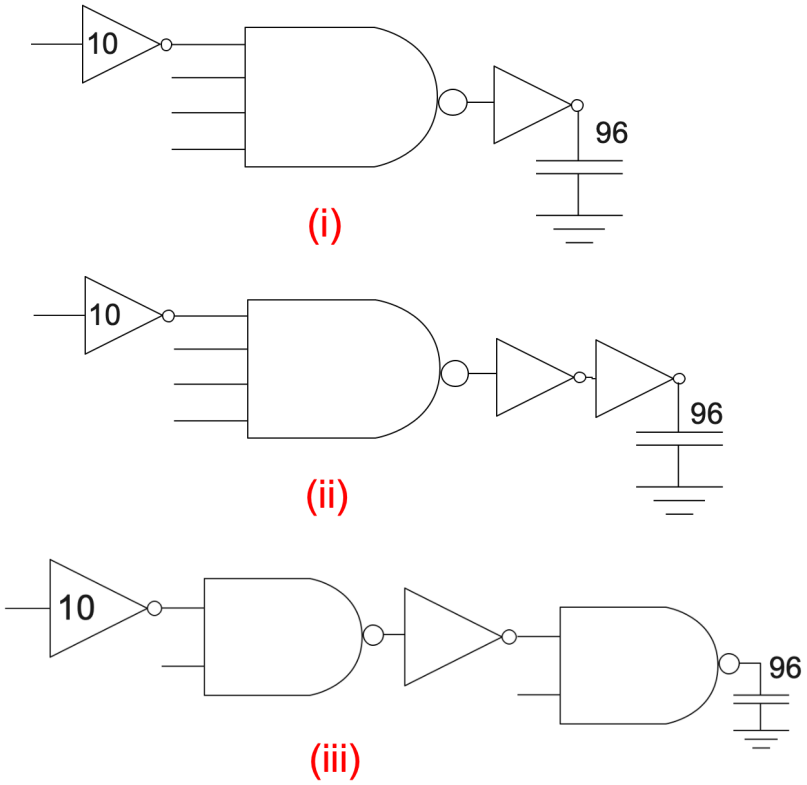
a) 0
b) 1
c) 2
d) 3
e) 4
f) 5
g) 6
h) 7

Solution = Ln(1927)/Ln(3.591)=5.91. current design already has six stages. No need to add additional stages.

9. For an inverter with input capacitance of 8C, and load capacitance of 1024C, what is the optimum number of inverter stages including the first one required to minimize the delay keeping the non-inverted logic.

a) 1
b) 10
c) 2
d) 4
e) 3
f) $2\sqrt{2}$
g) 3.7
h) 3.59

10. Examine circuits i, ii, and iii and organize them in the correct order based on their respective critical path delays.



a) (i) > (ii) > (iii)
b) (i) > (iii) > (ii)
c) (ii) > (i) > (iii)
d) (ii) > (iii) > (i)
e) (iii) > (i) > (ii)
f) (iii) > (ii) > (i)
g) (i) > (iii) = (ii)
h) (i) < (iii) = (ii)