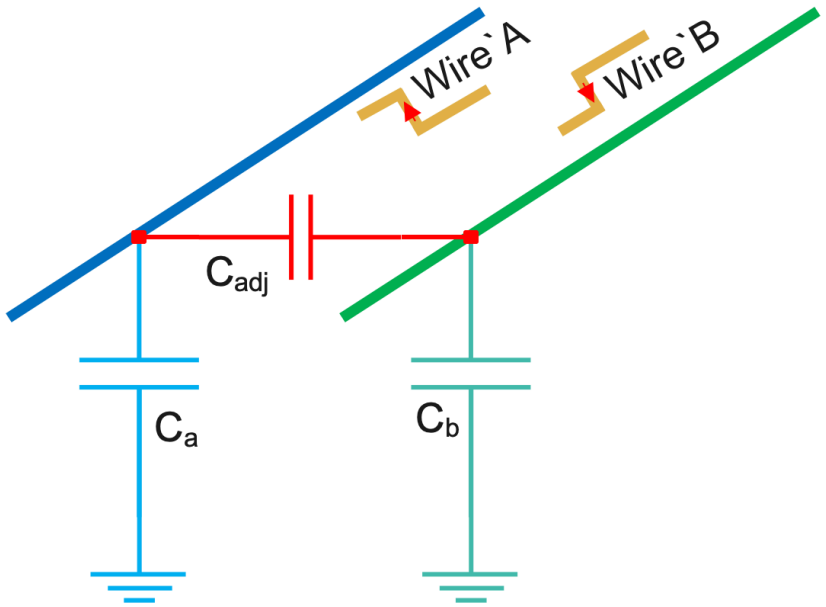
Week 8

1. In a digital circuit, consider two parallel wires, A and B, with respective capacitances Ca and Cb, and a capacitance Cadj between them. Wire A switches from 0 to Vdd, while Wire B switches from Vdd to 0. Determine the effective capacitance seen by Wire A during this transition and calculate the resulting charge Q.

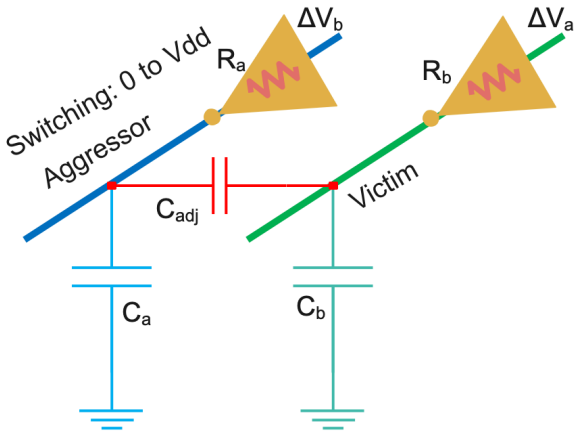


a) Ceff = Ca+Cadj; Q= (Ca+Cadj).Vdd
b) Ceff = Ca; Q= (Ca).Vdd
c) Ceff = Cadj; Q= (Cadj).Vdd
d) Ceff = Ca+2.Cadj; Q= (Ca+2Cadj).Vdd
e) Ceff = Cb+Cadj; Q= (Cb+Cadj).Vdd
f) Ceff = Cb; Q= (Cb).Vdd
g) Ceff = 2Cadj; Q= (2.Cadj).Vdd
h) Ceff = Cb+2.Cadj; Q= (Cb+2Cadj).Vdd

2. Given the capacitances Ca and Cb of Wires A and B, along with inverters switching resistances Ra and Rb, and assuming the absence of parasite capacitances of inverters and resistance of wires, explore the impact on Wire B when Aggressor undergoes a switching transition from 0 to Vdd. Address the following cases and identify the change in voltage in Wire B:

(i) If the driver and aggressor have the same widths.
(ii) In the scenario where the victim wire is floating, experiencing no driving inverter.
(iii) When the victim is driven by an inverter that is half the size of inverter A.

(iv) When the victim is driven by an inverter that is double the size of inverter A.



a) (i) 16.6% of ΔVa = ΔVb; (ii) 50% of ΔVa = ΔVb; (iii) 25% of ΔVa = ΔVb; (iv) 10% of ΔVa = ΔVb;
b) (i) 50% of ΔVa = ΔVb;(ii) 16.6% of ΔVa = ΔVb; (iii) 25% of ΔVa = ΔVb; (iv) 10% of ΔVa = ΔVb;
c) (i) 10% of ΔVa = ΔVb;(ii) 25% of ΔVa = ΔVb; (iii) 50% of ΔVa = ΔVb; (iv) 16.6% of ΔVa = ΔVb;
d) (i) 25% of ΔVa = ΔVb;(ii) 10% of ΔVa = ΔVb; (iii) 16.6% of ΔVa = ΔVb; (iv) 50% of ΔVa = ΔVb;
e) (i) 50% of ΔVa = ΔVb;(ii) 16.6% of ΔVa = ΔVb; (iii) 10% of ΔVa = ΔVb; (iv) 25% of ΔVa = ΔVb;
f) (i) 16.6% of ΔVa = ΔVb; (ii) 25% of ΔVa = ΔVb; (iii) 10% of ΔVa = ΔVb; (iv) 50% of ΔVa = ΔVb;
g) (i) 10% of ΔVa = ΔVb;(ii) 50% of ΔVa = ΔVb; (iii) 16.6% of ΔVa = ΔVb; (iv) 25% of ΔVa = ΔVb;
h) (i) 25% of ΔVa = ΔVb;(ii) 10% of ΔVa = ΔVb; (iii) 50% of ΔVa = ΔVb; (iv) 16.6% of ΔVa = ΔVb;

3. Considering two adjacent wires that are designed with coupling capacitance of 0.14 pF/µm, and length of both wires are 1mm. The wires are characterized to 0.08fF/µm, and driver gate resistance for the wire is 1 K-Ohm, what is the propagation delay for the signal in one of the wires ?

a) 160 ps
b) 480 ps
c) 320 ps
d) 360 ps
e) 500 ps
f) 340 ps
g) 160 ps
h) 80 ps

4. Determine the proportionality factors of the RC delay for a wire with length "L" under different scenarios:

x) The RC delay of a wire without repeaters is proportional to factor X.
y) The RC delay of a wire with a fixed number of repeaters "F" is proportional to factor Y.
z) The RC delay of a wire with a variable number of repeaters N (where N increases proportionally with length) is proportional to factor Z.

Identify the correct proportionality factors X, Y, and Z from the given options.

a)	X: L^2	Y: (L/F)^2	Z: L
b)	X: L^3	Y: (L/F)^3	Z: L^2
c)	X: L^2	Y: (L/F)^2	Z: L^2
d)	X: L	Y: (L/F)^2	Z: L^2
e)	X: L^2	Y: (L/F)^3	Z: L/N
f)	X: L^2	Y: (L/F)^2	Z: L/(N^2)
g)	X: L^2	Y: (L^2)/F	Z: L
h)	X: L^2	Y: (L^3)/(F^2)	Z: L

5) For an interconnect utilizing inverters as repeaters, given an interconnect resistance (Rw) of 300 Ohm/mm, interconnect capacitance (Cw) of 0.1fF/mm, and the switching resistance (R) and parasitic capacitance (C) of each inverter as 15KOhm and 0.3fF respectively, what is the optimal width of repeaters that minimizes delay? (Consider 65nm technology node)

a) 1 x 100 nm
b) 8.25 x 100 nm
c) 2.264 x 100 nm
d) 1.29 x 100 nm
e) 4.08 x 100 nm
f) 0.08164 x 100 nm
g) 0.258 x 100 nm
h) 12247.448 x 100 nm

Solution:

W=Sqrt(RCw/RwC)
R=15k, C=0.3fF, Rw=300, Cw=0.1fF
Sqrt { (15000 * 0.1) / (300 * 0.3) } = 4.08

6) In an interconnect design employing inverters as repeaters, where the interconnect parameters include a resistance (Rw) of 500 Ohm/mm and capacitance (Cw) of 0.6fF/mm, and the switching resistance (R), parasitic capacitance (C), and normalized parasitic factor of each inverter are specified as 10KOhm, 0.3fF, and 0.5 respectively, determine the optimal length(in mm) of each interconnect segment for minimal delay.

a) 10.95
b) 0.42
c) 5.47
d) 0.54
e) 1.73
f) 2.46
g) 3.92
h) 7.69

Solution:
(L/N)@min delay = Sqrt{ 2RC.(1+ρ)/RwCw }

R=10k, C= 0.3, ρ=0.5, Rw=500, Cw=0.6
L/N = Sqrt{ 2*10000*0.3*(1+0.5)/500*0.6 }=5.477mm

7) Consider an interconnect featuring inverters as repeaters with a resistance of 100 Ohms per mm and a capacitance of 0.1 fF per milli-meter length. Each inverter, designed with folded technology, exhibits an FO4 delay of 20 ps. With a nominal voltage of 1 volt, estimate the propagation delay per unit length and the energy of a bit per unit length for the wire.

a) Tpd/l = 23.6ps, E/l=0.1863pJ/mm
b) Tpd/l = 23.6us, E/l=0.1863pJ/mm
c) Tpd/l = 23.6us, E/l=0.1863uJ/mm
d) Tpd/l = 2.36ps, E/l=1.863pJ/mm
e) Tpd/l = 47.2us, E/l=1.863pJ/mm
f) Tpd/l = 52.6us, E/l=1.863pJ/mm
g) Tpd/l = 54.7us, E/l=1.863pJ/mm
h) Tpd/l = 12.9us, E/l=1.863pJ/mm

Solution:
Rw=100, Cw=0.1, FO4=5RC=20 => RC=4, ρ=0.5
tpd/l=Sqrt(RwCwRC) . (2+ Sqrt(2.(1+ ρ))

$\sqrt{100\times0.1\times10^{-12}\times4\times10^{-12}}\times(2+\sqrt{3})$ = 23.6ps

E/l=1.866.Cw.Vdd^2=1.866*0.1*1^2=0.1863pJ/mm

8) Identify the false statements:

(i) To reduce cross talk, Victim driver size should be reduced.
(ii) Folded technology has less parasitic capacitance because of shared diffusion, normalized parasitic factor becomes " 0.5".
(iii) Repeaters help to reduce delay of wires.
(iv) Interconnect with repeaters tuned for optimal delay consume more energy.
(v) The Delay per unit length profile of a repeater circuit exhibits a parabolic trend in relation to the width parameter (w).

(vi) The Delay per unit length profile of a repeater circuit exhibits a linear trend in relation to the width parameter (w).

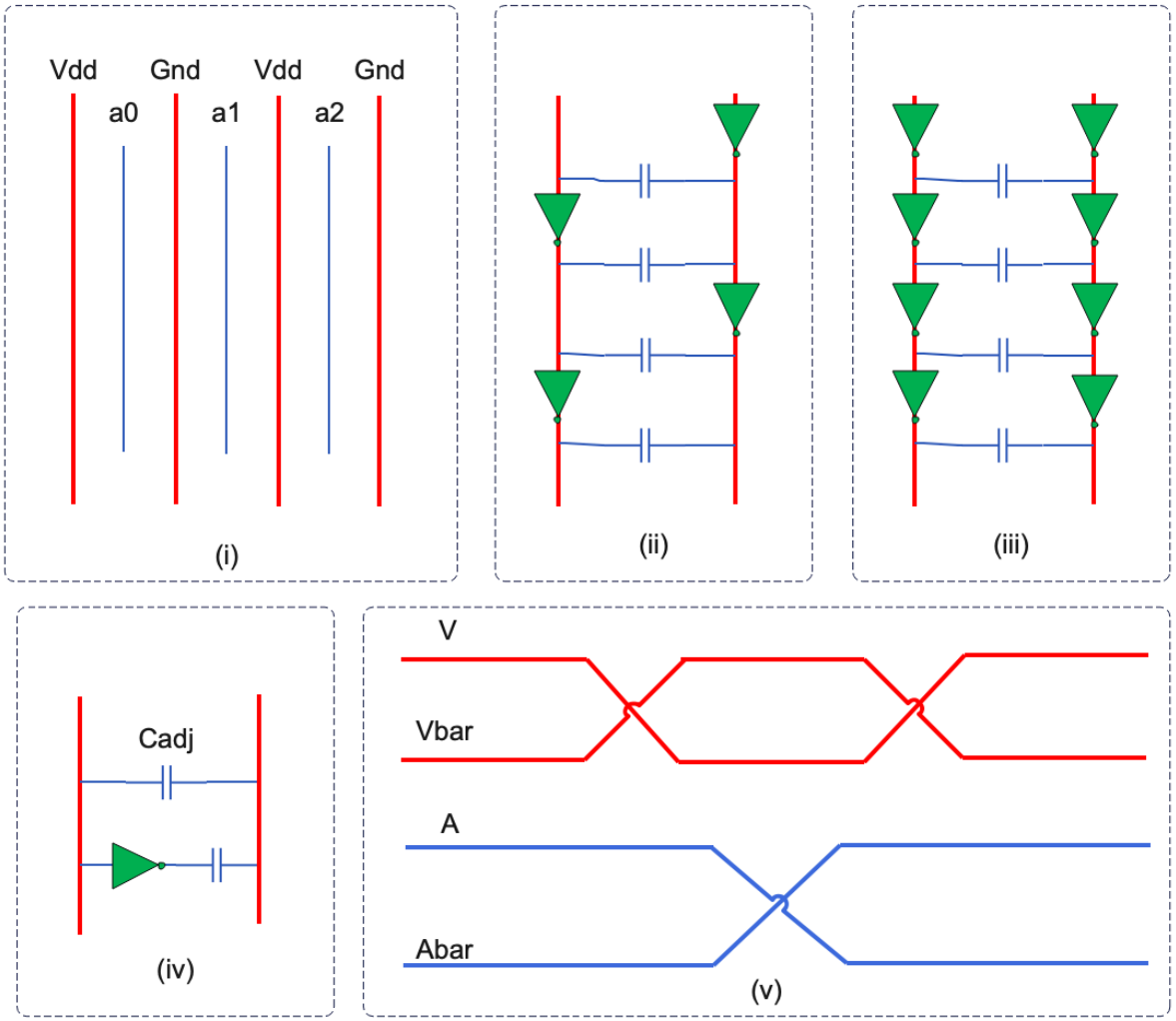
(vii) The Energy per unit length profile of a repeater circuit exhibits a parabolic trend in relation to the width parameter (w).

(viii) The Energy per unit length profile of a repeater circuit exhibits a linear trend in relation to the width parameter (w).

(ix) Repeaters helps to avoid signal attenuation.

a) iii,vi, vii
b) iii, v,viii
c) ii,vi, vii
d) ii, v,viii
e) i, v,viii
f) i, vi, vii
g) iv,vi, vii
h) ix, v,viii

9) Match the Cross talk control schemes
(p) Shielding of wires
(q) Staggered Repeaters
(r) Charge Compensation
(s) Twisted Differential Signalling



a) p:i q:iii r:iv s:v
b) p:ii q:i r:iv s:v
c) p:i q:ii r:iv s:v
d) p:ii q:iii r:iv s:v
e) p:i q:iii r:v s:iv
f) p:v q:ii r:iii s:iv
g) p:iii q:ii r:iv s:v
h) p:v q:iii r:iv s:ii

10. Identify Correct statements.

(i) When input transitioning from 0 to Vdd in an inverter, the output voltage follows a linear profile while decreasing from Vdd to Vdd-Vt.
(ii) When input transitioning from 0 to Vdd in an inverter, the output voltage exhibits an exponential profile while decreasing from Vdd-Vt to 0.
(iii) When input transitioning from 0 to Vdd in an inverter, the discharging current exhibits a constant value while decreasing from Vdd to Vdd-Vt.
(iv) When transitioning from 0 to Vdd in an inverter, the current profile displays an exponential behavior during the output voltage range from Vdd-Vt to 0
(v) Area under charging power profile is equal to discharging power profile.

(vi) When input transitioning from 0 to Vdd in an inverter, the output voltage follows a linear profile while decreasing from Vdd to Vt.

(vii) When input transitioning from 0 to Vdd in an inverter, the output voltage exhibits an parabolic profile while decreasing from Vt to 0.

(viii) When input transitioning from 0 to Vdd in an inverter, the discharging current exhibits a constant value while decreasing from Vdd to Vt.

(ix) When transitioning from 0 to Vdd in an inverter, the current profile displays an parabolic behavior during the output voltage range from Vt to 0

(x) When input transitioning from Vdd to 0 in an inverter, the output voltage follows a exponential profile while increasing from 0 to Vdd-Vt.

(xi) When input transitioning from Vdd to 0 in an inverter, the output voltage exhibits an linear profile while increasing from 0 to Vdd-Vt.

(xii) When input transitioning from Vdd to 0 in an inverter, the discharging current exhibits a constant value while increasing from Vdd-Vt to 0.

(xiii) When transitioning from Vdd to 0 in an inverter, the current profile displays an exponential behavior during the output voltage range from 0 to Vdd-Vt

a) i,ii,iii,iv,v
b) v,vi,vii,viii,ix
c) v,x,xi,xii,xiii
d) i,ii,iii,iv
e) vi,vii,viii,ix
f) x,xi,xii,xiii
g) i,ii,v,xii,xiii
h) v,vii,viii,x,xi