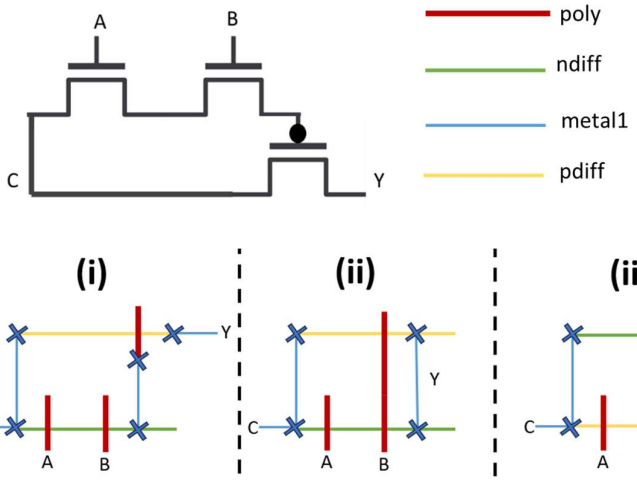
Week -7

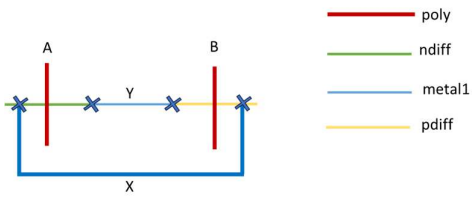
1) For a 2-NOR (2 input NOR gate), what is the footprint of the gate designed to match 2:1 inverter rising and falling resistances? [HINT – Use Stick diagram]
   a) 42 ʎ × 12 ʎ
   b) 48 ʎ × 24 ʎ
   c) 52 ʎ × 24 ʎ
   d) 48 ʎ × 12 ʎ
   e) 48 ʎ × 36 ʎ
   f) 48 ʎ × 56 ʎ
   g) 56 ʎ × 48 ʎ
   h) 50 ʎ × 40 ʎ

2) Which of the following stick diagram represents the circuit diagram.



   a) (i)
   b) (ii)
   c) (iii), (iv)
   d) (i), (ii), (iii)
   e) (i), (iii)
   f) (i), (iv)
   g) (ii), (iii)
   h) (iii)

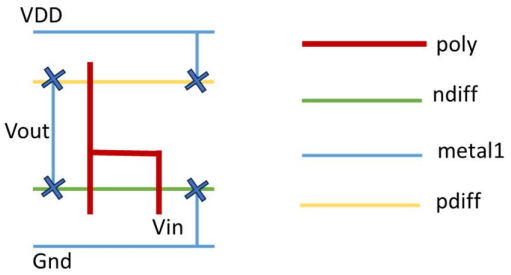
3) The stick diagram represents a



   a) NAND gate
   b) NOR gate
   c) Tristate Buffer

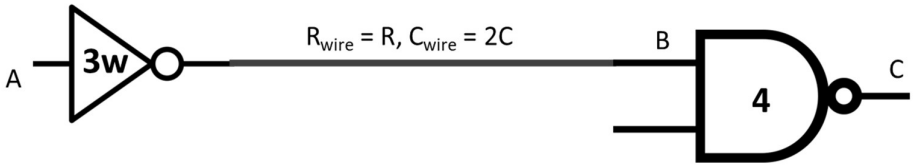
d) Two cascaded pass transistors
e) Tristate Inverter
f) Transmission gate with A=enable, B=enable' , X, Y as IN and OUT interchangeably
g) Cascaded Inverters
h) Common Stage amplifier

4) The given stick diagram below functionally behaves as



a) Pass Transistor
b) Tristate Buffer
c) Transmission Gate
d) Tristate Inverter
e) Domino NOR
f) Domino NAND
g) Buffer
h) Inverter

5) Considering π model for the interconnect, the delay from A to B is



a) 8RC + 7RC/w
b) 5RC + RC/w
c) 8RC + 6RC/w
d) 5RC + 2RC/w
e) RC + 3RC/w
f) RC + 5RC/w
g) 9RC + RC/w
h) 9RC + 8RC/w

6) Die of 20 mm ×20 mm running at 4GHz in 65 nm process with pitch of 250 nm. Half of the available wire tracks are used. Wire activity factor α = 0.2, Cw = 0.3pF/mm. What is the total interconnect capacitance? Also, find the switching power.(Assume Vdd = 1V)
a) 160nF, 230W
b) 280nF, 480W
c) 360nF, 800W
d) 330nF, 560W
e) 240nF, 192W

f) 220nF, 180W
g) 210nF, 150W
h) 136nF, 55W

7) In a compact layout for a 3-input NAND gate with P:N sizes as 2:3, what is the parasitic capacitance seen at the output node? Also, find its falling contamination delay.
   a) 2C, 2RC
   b) 3C, 3RC
   c) 5C, 5RC
   d) 15C, 15RC
   e) 12C, 12RC
   f) 6C, 6RC
   g) 7C, 7RC
   h) 9C, 9RC

8) To For a 2-NAND (2 input NAND gate), what is the footprint of the gate designed to match 2:1 inverter rising and falling resistances? [HINT – Use Stick diagram]
   a) 42 ʎ × 12 ʎ
   b) 54 ʎ × 24 ʎ
   c) 24 ʎ × 48 ʎ
   d) 52 ʎ × 24 ʎ
   e) 48 ʎ × 48 ʎ
   f) 24 ʎ × 56 ʎ
   g) 56 ʎ × 48 ʎ
   h) 50 ʎ × 40 ʎ

9) As In a compact layout for a 3-input NOR gate with P:N sizes as 6:1, what is the parasitic capacitance seen at the output node ? Also, what is its falling contamination delay?
   a) 1C, 1RC
   b) 6C, 6RC
   c) 7C, 7RC
   d) 18C, 18RC
   e) 3C, 3RC
   f) 21C, 21RC
   g) 8C, 8RC/3
   h) 9C, 9RC

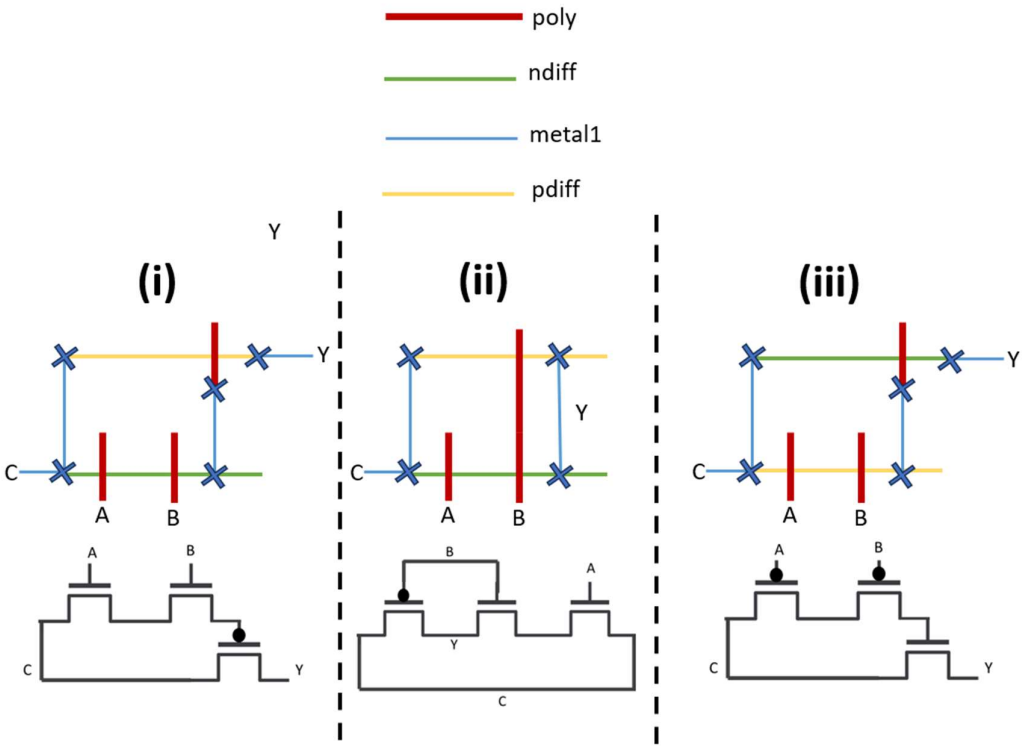
10) Hypothetically, if the length of the interconnect is doubled, the width of the interconnect is tripled and the thickness of the interconnect is halved, the resistance R and the sheet resistance R□ become
   a) 4R/3 and R□/2
   b) 3R/4 and R□/2
   c) 3R/4 and 2R□
   d) 4R/3 and R□
   e) 2R and 4R□/3
   f) 4R/3 and 2R□

g) 5R/3 and R□
h) 5R/3 and R□/3

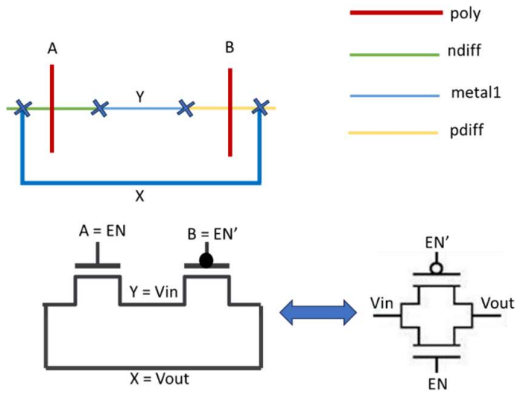
Solution:

1) **c) 52λ x 24λ**
Width = 5 x 8λ + 3 x 4λ
Length = 3 x 8λ

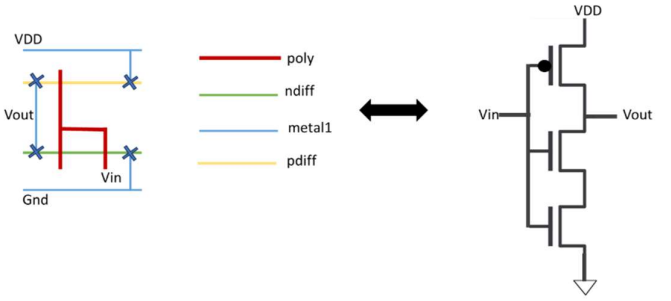
2) **a) (i)**
The corresponding circuits are:



3) **f) Transmission gate with A=enable, B=enable' , X, Y as IN and OUT interchangeably**

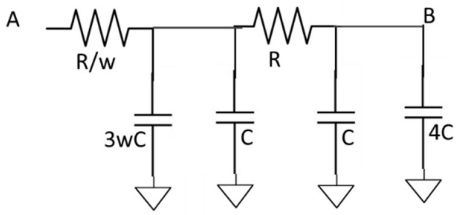


4) **h) Inverter**



So, the circuit essentially behaves as an inverter.

5) **c) 8RC + 6RC/w**



Applying the elmore delay model, we get

tpd = $\frac{R}{w}$ x (3wC + C) + ($\frac{R}{w}$+R) x 5C = 3RC + $\frac{RC}{w}$ + $\frac{5RC}{w}$ + 5RC = **8RC + 6RC/w**

6) **e) 240nF, 192W**

Number of wires = 20mm/250nm = 80 x 10^3

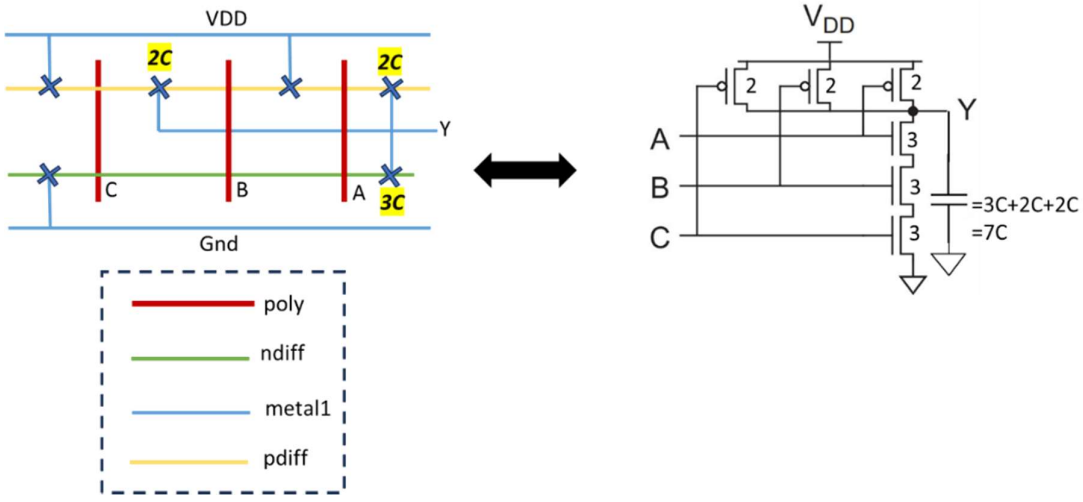
Half of the wire tracks are used = N = 80000/2 = 40000

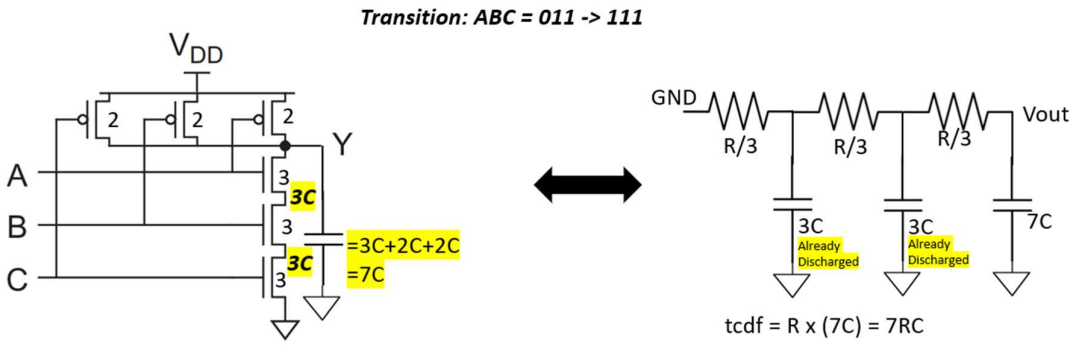
C_{wire} = 40000 x 0.3 x 20 = 240nF

Evdd = $\alpha C_{wire} Vdd^2$ = 48nJ

Power = Evdd x freq = 48nJ x 4GHz = 192W

7) **g) 7C, 7RC**



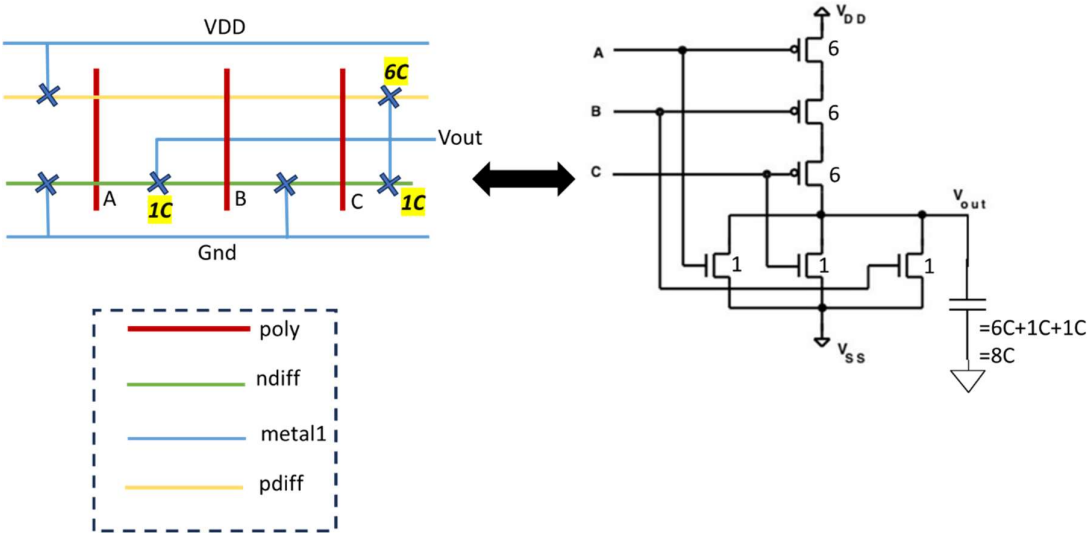


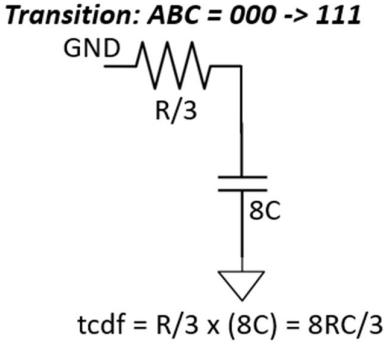
8) **c) 24λ x 48λ**

Width = 5 x 8λ + 4λ + 4λ

Length = 3 x 8λ

9) **g) 8C, 8RC/3**





10) **f) 4R/3 and 2R□**

$R\square = \rho/t$. If ***t*** is halved, $R\square_{new} = 2\ R\square$.

Now,

$R_{new} = R\square_{new} \times l_{new}/w_{new} = 2\ R\square \times 2l/3w = 4R/3$