Week: 11

1. Pick Correct Maximum delay constraints for respective logical block.
   ($T_{pw} < T_{setup}$).
   a) Flipflop: $T_{pd} \leq T_c - T_{ccq} - T_{setup}$; Latch: $T_c / 2 \leq T_{pdq} + T_{pd}$; PulseLatch($T_{pw} < T_{setup}$): $T_{pcq} - T_{pd} + T_{setup} - T_{pw} \leq T_c$; PulseLatch($T_{pw} > T_{setup}$): $T_{pdq} - T_{pd} \geq T_c$;
   b) Flipflop: $T_{pd} \leq T_c - T_{pd} - T_{setup}$; Latch: $T_c / 2 \leq T_{pdq} + T_{pd}$; PulseLatch($T_{pw} < T_{setup}$): $T_{pcq} - T_{pd} - T_{setup} - T_{pw} \leq T_c$; PulseLatch($T_{pw} > T_{setup}$): $T_{pdq} + T_{pd} \leq T_c$;
   c) Flipflop: $T_{pd} \leq T_c + T_{pcq} - T_{setup}$; Latch: $T_c / 2 \geq T_{pdq} - T_{pd}$; PulseLatch($T_{pw} < T_{setup}$): $T_{pcq} - T_{pd} - T_{setup} + T_{pw} \leq T_c$; PulseLatch($T_{pw} > T_{setup}$): $T_{pdq} - T_{pd} \geq T_c$;
   d) Flipflop: $T_{pd} \leq T_c - T_{pcq} + T_{setup}$; Latch: $T_c / 2 \leq T_{pdq} - T_{pd}$; PulseLatch($T_{pw} < T_{setup}$): $T_{pcq} - T_{pd} + T_{setup} + T_{pw} \leq T_c$; PulseLatch($T_{pw} > T_{setup}$): $T_{pdq} + T_{pd} \leq T_c$;
   e) Flipflop: $T_{pd} \leq T_c - T_{pcq} - T_{setup}$; Latch: $T_c / 2 \geq T_{pdq} + T_{pd}$; PulseLatch($T_{pw} < T_{setup}$): $T_{pcq} + T_{pd} + T_{setup} - T_{pw} \leq T_c$; PulseLatch($T_{pw} > T_{setup}$): $T_{pdq} + T_{pd} \leq T_c$;
   f) Flipflop: $T_{pd} \geq T_c - T_{pcq} - T_{setup}$; Latch: $T_c \geq T_{pdq} + T_{pd}$; PulseLatch($T_{pw} < T_{setup}$): $T_{pcq} + T_{pd} - T_{setup} + T_{pw} \leq T_c$; PulseLatch($T_{pw} > T_{setup}$): $T_{pdq} - T_{pd} \geq T_c$;
   g) Flipflop: $T_{pd} \geq T_c + T_{pcq} - T_{setup}$; Latch: $T_c / 2 \geq T_{pdq} + T_{pd}$; PulseLatch($T_{pw} < T_{setup}$): $T_{pcq} + T_{pd} + T_{setup} - T_{pw} \geq T_c$; PulseLatch($T_{pw} > T_{setup}$): $T_{pdq} + T_{pd} \leq T_c$;
   h) Flipflop: $T_{pd} \leq T_c + T_{pcq} + T_{setup}$; Latch: $T_c \leq T_{pdq} + T_{pd}$; PulseLatch($T_{pw} < T_{setup}$): $T_{pcq} - T_{pd} + T_{setup} + T_{pw} \geq T_c$; PulseLatch($T_{pw} > T_{setup}$): $T_{pdq} - T_{pd} \geq T_c$;

2. Pick Correct Minimum delay constraints for respective logical block.
   a) PulseLatch: $T_{hold} \geq T_{cd} + T_{pw} - T_{ccq}$; Latch: $T_{nonoverlap} - T_{cd} + T_{ccq} \geq T_{hold}$; Flipflop: $T_{hold} \leq T_{cd} - T_{ccq}$
   b) PulseLatch: $T_{hold} \leq T_{cd} - T_{pw} + T_{ccq}$; Latch: $T_{nonoverlap} + T_{cd} + T_{ccq} \geq T_{hold}$; Flipflop: $T_{hold} \leq T_{cd} + T_{ccq}$
   c) PulseLatch: $T_{hold} \geq T_{cd} - T_{pw} + T_{ccq}$; Latch: $T_{nonoverlap} + T_{cd} - T_{ccq} \geq T_{hold}$; Flipflop: $T_{hold} \geq T_{cd} + T_{ccq}$
   d) PulseLatch: $T_{hold} \leq T_{cd} - T_{pw} - T_{ccq}$; Latch: $T_{nonoverlap} - T_{cd} - T_{ccq} \geq T_{hold}$; Flipflop: $T_{hold} \geq T_{cd} - T_{ccq}$
   e) PulseLatch: $T_{hold} \leq T_{cd} + T_{pw} + T_{ccq}$; Latch: $T_{nonoverlap} + T_{cd} + T_{ccq} \leq T_{hold}$; Flipflop: $T_{hold} \leq T_{cd} - T_{ccq}$
   f) PulseLatch: $T_{hold} \geq T_{cd} - T_{pw} - T_{ccq}$; Latch: $T_{nonoverlap} - T_{cd} + T_{ccq} \leq T_{hold}$; Flipflop: $T_{hold} \leq T_{cd} + T_{ccq}$
   g) PulseLatch: $T_{hold} \geq T_{cd} - T_{pw} - T_{ccq}$; Latch: $T_{nonoverlap} + T_{cd} - T_{ccq} \leq T_{hold}$; Flipflop: $T_{hold} \geq T_{cd} - T_{ccq}$

h) Flipflop: $T_{hold} \leq T_{cd} + T_{pw} - T_{ccq}$; Latch: $T_{nonoverlap} - T_{cd} - T_{ccq} \leq T_{hold}$;
Flipflop: $T_{hold} \geq T_{cd} - T_{ccq}$

3. What is the setup time for a CMOS Latch standard cell design if the inverter and gates used in the design is characterized for 5 ps, and 20 ps propagation delay respectively? Note that CMOS Latch forward path is made up of an Inverter-TransmissionGate-Inverter.

a) 5 ps
b) 21 ps
c) 15 ps
d) 20 ps
e) 10 ps
f) 40 ps
g) 25 ps
h) 30 ps

4. What is the setup time for a CMOS flipflop standard cell design if the inverter and transmission gates used in the design is characterized for 15 ps, and 20 ps respectively? Note that the forward path of the first latch is composed of Inverter-TransmissionGate-Inverter design.

a) 100 ps
b) 50 ps
c) 15 ps
d) 20 ps
e) 30 ps
f) 40 ps
g) 10 ps
h) 70 ps

5. What should be the minimum clock time-period for a sequential data-path subsystems consisting of a 32-bit adder subsystem in between two flops to avoid setup time failure ? The setup time of flop is 52 ps, propagation clock to output of flop is 100 ps, and propagation delay of 32-bit adder subsystem is 590 ps.

a) 100 ps
b) 152 ps
c) 590 ps
d) 742 ps
e) 690 ps
f) 642 ps
g) 102 ps
h) 642 ps

6. What should be the minimum contamination delay that is acceptable for the 32-bit adder subsystem which is in-between two flops to avoid hold-time failure ? The contamination delay for the flop is characterized to 5 ps, and hold time of the flop is 100 ps.

a) 96 ps
b) 29 ps
c) 15 ps
d) 31 ps
e) 19 ps
f) 19 ps
g) 6 ps
h) 5 ps

7. For a combinational circuit datapath subsystem consisting of 32-bit adder, and 32:1 Multiplexer in between two flops where first flop is positive edge triggered, and second flop is negative edge triggered, what should be the 32:1 multiplexer propagation and contamination delay respectively to avoid setup time and hold time failure considering the following parameters. Assume that the clock is having equal ON (HIGH) and OFF (LOW) time.

T_{pcq} for flops	90 ps
T_{setup} for flops	62 ps
T_{ccq} for flops	75 ps
T_{hold} for flops	10 ps
T_{pd} for Adder	590 ps
T_{cd} for Adder	100 ps
T_{clock}	1000 ps

a) 300 ps & 330 ps
b) 330 ps & 300 ps
c) 63 ps & 9 ps
d) 63 ps & 11 ps
e) 745 ps & 340 ps
f) 1100 ps & 300 ps
g) 849 ps & 334 ps
h) 849 ps & 336 ps

8. For a combinational datapath subsystem consisting of 32-bit adder, and a buffer design in between two pulsed latch, which buffer design with the stated propagation and contamination delay, avoids the setup-time and hold-time failure considering the following parameters:

T_{pcq}	82 ps
T_{pdq}	92 ps
T_{setup}	40 ps
T_{ccq}	52 ps
T_{hold}	25 ps
T_{pd} for Adder	590 ps
T_{cd} for Adder	100 ps
T_{pw}	30 ps
T_{clock}	1000 ps

a) 400 ps & 330 ps
b) 500 ps & 300 ps
c) 1001 ps & 9 ps
d) 319 ps & 11 ps
e) 325 ps & 340 ps
f) 310 ps & 5 ps
g) 849 ps & 334 ps
h) 849 ps & 336 ps

9. For a combinational circuit datapath subsystem consisting of 32-bit adder, and buffer design in between two flops where both flops are positive edge triggered what should be the buffer design propagation and contamination delay respectively to avoid setup time and hold time failure considering the following parameters, with a clock characterized to have skewing effect:

T_{pcq} for flops	90 ps
T_{setup} for flops	62 ps
T_{ccq} for flops	10 ps
T_{hold} for flops	10 ps
T_{pd} for Adder	590 ps
T_{cd} for Adder	15 ps
T_{clock}	1000 ps
t_{skew}	40 ps

a) 200 ps & 80 ps
b) 330 ps & 60 ps
c) 200 ps & 9 ps
d) 63 ps & 11 ps
e) 1001 ps & 340 ps
f) 219 ps & 300 ps
g) 849 ps & 24 ps
h) 849 ps & 24 ps

10. For a standard cell library design for an asynchronous CLEAR and SET enabled Flipflop design, what is the transistor count?

a) 200
b) 240
c) 340
d) 160
e) 12
f) 180
g) 80
h) 28