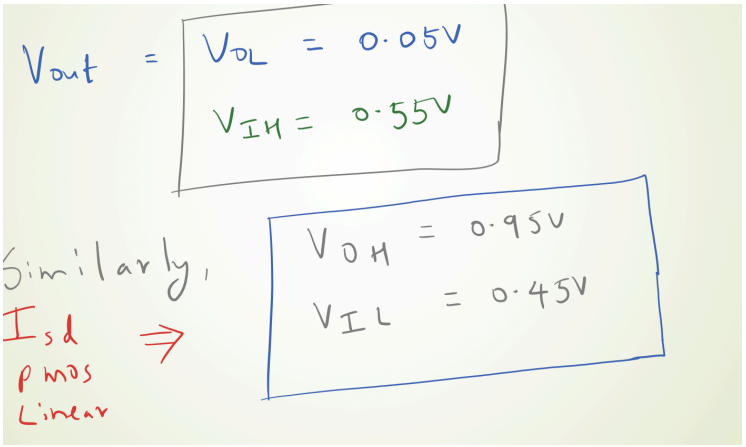
NPTEL Assignment
Week-3

1. Select Correct statements from the following statements:
i) The Noise margin corresponding to the higher voltage level is defined as $NM_H = V_{OH} - V_{IH}$
ii) The Noise margin corresponding to the higher voltage level is defined as $NM_H = V_{IH} - V_{OH}$
iii) The Noise margin corresponding to the lower voltage level is defined as $NM_L = V_{OL} - V_{IL}$
iv) The Noise margin corresponding to the lower voltage level is defined as $NM_L = V_{IL} - V_{OL}$

1. Only i, ii, iii
2. Only i
3. Only ii, iii
4. Only iv
5. **Only i, iv**
6. Only iii
7. Only i, iii
8. All of the above

2. For an unskewed inverter of size 4:2 as P:N, what is the NM_H and NM_L value for a 65 nm technology node with rail voltage of 1V ?

1. 100,100 mV
2. 50,50 mV
3. 550,550 mV
4. 500,500 V
5. 400,450 V
6. 450,400 mV
7. 450,500 mV
8. **400,400 mV**



Solution:-

3. If the inverter circuit for a rail voltage of 1V is characterized to have noise signal below 0.5V with ideally zero static current, and no overhead clock signal, the designers are likely to use the following designs?

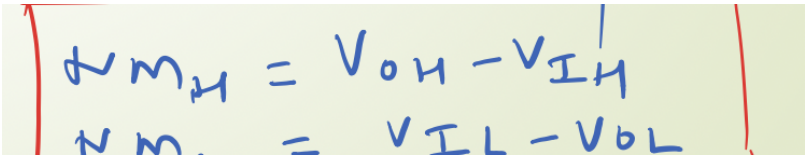
1. **High-Skew Inverter**
2. Low-Skew Inverter
3. 2:1 Un-skewed Inverter
4. Higher Widths of Un-skewed Inverter
5. Asymmetric design
6. Pseudo NMOS Inverter
7. Dynamic Inverter
8. Transmission gate based inverter

4. Select correct ones from the following statements:
i) As the skew ratio, γ increases, NML decreases and NMH increases.
ii) As the skew ratio, γ increases, NML increases and NMH decreases.
iii) As the skew ratio, γ decreases, NML decreases and NMH increases.
iv) As the skew ratio, γ decreases, NML increases and NMH decreases.

1. Only i, ii, iii
2. Only i
3. **Only ii, iii**
4. Only iv
5. Only ii, iv
6. Only iii
7. Only i, iii
8. All of the above

5. A particular logic family has VOH = 5 V, VOL = 1 V, VIH = 3.5 V and VIL = 2 V. The noise margin values NMH and NML will be

1. **1.5V,1V**
2. 2V,1V
3. 0.5V,1V
4. 1V,1V
5. 1V,1.5V
6. 1.5V,1.5V
7. 2V,2V
8. 0.5V,0.5V

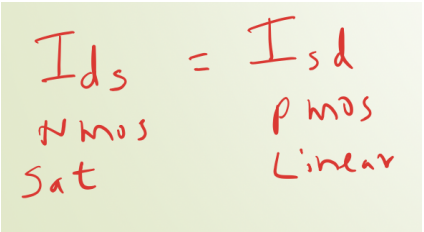


Solution:-

6. Find VOH and VIL for an ideal transistor given the following metrics:

βNMOS = βPMOS
VDD = 1V
Vt,PMOS = -0.3V
Vt,NMOS = 0.3V

1. VOH = 0.75V VIL = 0.45V
2. VOH = 0.65V VIL = 0.45V
3. **VOH = 0.95V VIL = 0.45V**
4. VOH = 0.9V VIL = 0.45V
5. VOH = 0.95V VIL = 0.15V
6. VOH = 0.95V VIL = 0.25V
7. VOH = 0.95V VIL = 0.35V
8. VOH = 0.85V VIL = 0.45V



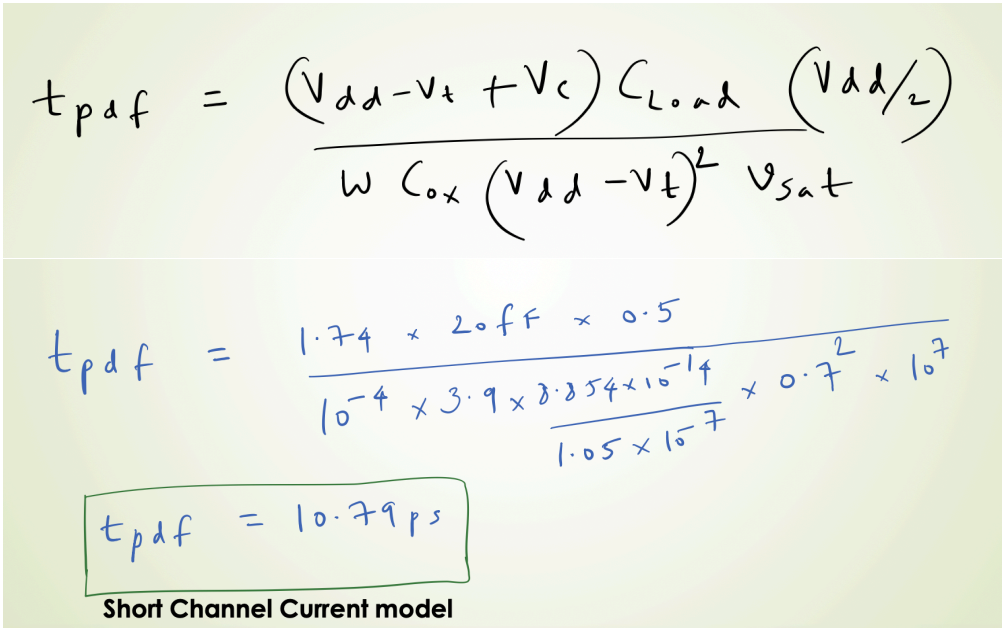
Solution:-

7. For 65 nm technology node,
W = 1μm

L = 50nm
tox = 1.05nm
εox = 3.9 x 8.854 x 10-14 F/cm
CLoad = 20 fF
VDD = 1V
Vt,PMOS = -0.3V
Vt,NMOS = 0.3V
Vdt = VDD - Vt
Saturation velocity for nMOS = 107 cm/s
Vc = 1.04V
μ = 80cm2/v-sec and short channel model. Find tpdf.

1. tpdf = 5.79ps
2. tpdf = 5.22ps
3. tpdf = 8.66ps
4. tpdf = 7.24ps
5. **tpdf = 10.79ps**
6. tpdf = 8.01ps
7. tpdf = 6.76ps
8. tpdf = 11.98ps

Solution:-



8. For k = 2, the Switching resistances and diffusion capacitances are(R = switching resistance of unit NMOS; C = diffusion capacitance of unit NMOS):

1. RNMOS = R/4; RPMOS = R/2; CNMOS = C/4; CPMOS = C/2
2. RNMOS = R/2; RPMOS = R/4; CNMOS = C/2; CPMOS = C/4
3. RNMOS = 4R; RPMOS = 2R; CNMOS = 4C; CPMOS = 2C
4. RNMOS = 2R; RPMOS = 4R; CNMOS = 2C; CPMOS = 4C
5. **RNMOS = R/2; RPMOS = R; CNMOS = 2C; CPMOS = 2C**

6. RNMOS = R/2; RPMOS = R/4; CNMOS = 2C; CPMOS = 2C
7. RNMOS = 4R; RPMOS = 2R; CNMOS = C/4; CPMOS = C/4
8. RNMOS = 2R; RPMOS = 4R; CNMOS = C/2; CPMOS = C/2

9. For Switching resistance = 2KΩ, Capacitance = 20fF, what is the RC approximation delay?

1. 6.93ps
2. 13.86ns
3. 13.86ps
4. 27.72ms
5. **27.72ps**
6. 27.72ns
7. 13.86ms
8. 6.93ns

Solution:-

0.693*R*C

10. For 65 nm technology node,
W = 1µm
L = 50nm
tox = 1.05nm
εox = 3.9 x 8.854 x 10-14 F/cm
CLoad = 20 fF
VDD = 1V
Vt,PMOS = -0.3V
Vt,NMOS = 0.3V
Vdt = VDD - Vt
µ = 80cm2/v-sec and long channel model. Find tpdf.

1. tpdf = 7.72ns
2. **tpdf = 7.72ps**
3. tpdf = 7.72ms
4. tpdf = 15.44ps
5. tpdf = 15.44ns
6. tpdf = 15.44ms
7. tpdf = 3.86ps
8. tpdf = 3.86ns

Solution:-