Week -10

1) Why is tristate-inverter in the feedback path used in the CMOS Latch design?
   a) To reduce the sensitivity towards Output noise
   b) To reduce the sensitivity towards Input noise
   c) To avoid the Dynamic output
   d) To avoid Staticizing the output
   e) To get complete rail-to-rail output swing
   f) To improve the delay
   g) To improve the dynamic power
   h) To get benefits of dual logic family

2) In the most recommended Artisan Standard cell library design, a CMOS Latch has how many transistors?
   a) 100
   b) 500
   c) 110
   d) 200
   e) 140
   f) 1000
   g) 12
   h) 4

3) A chip is designed for 65nm technology library, which consists of the following parameters
   Number of Logic gates: 200×10^6, Width = 12λ, activity factor of logic gates = 0.1
   Number of gates used in Memory: 800×10^6, W = 4λ, activity factor of memory design=0.02
   Cgate = 1fF/μm, Cparasitic= 0.8 fF/μm.
   Estimate static power dissipated by the Vdd rail of 1V for the designed Chip.

Assumption:

i) Logic 95% low Vt cells, 5% high Vt cells

ii) Memory only low Vt cells

iii) Isub of low Vt cell is 100nA/μm and Isub of high Vt cell is 10nA/μm

iv) Operating Freq = 3GHz

   a) 9.9 mW
   b) 1000 W
   c) 1.185W
   d) 6.12 W
   e) 41.04
   f) W
   g) 18 mW
   h) 8 mW
   i) 28 mW

4) A chip is designed for 65nm technology library, which consists of the following parameters Number of Logic gates: 200×10^6, Width = 12λ, activity factor of logic gates = 0.1
Number of gates used in Memory: 800×10^6, W = 4λ, activity factor of memory design=0.02
Cgate = 1fF/μm, Cparasitic= 0.8 fF/μm. Estimate switching power dissipated by the Vdd rail of 1V for the designed Chip.

Assumption:

j) Logic 95% low Vt cells, 5% high Vt cells

ii) Memory only low Vt cells

iii) Isub of low Vt cell is 100nA/μm and Isub of high Vt cell is 10nA/μm

iv) Operating Freq = 3GHz

a) 9.9 mW
b) 1000 W
c) 1.185W
d) 6.12 W
e) 41.04 W
f) 18 mW
g) 8 mW
h) 28 mW

5) Evaluate the subthreshold-leakage current for 2-NAND gate when the inputs of 1, and 0 are applied. Consider Logic '1' to be applied to transistor closer to ground rail, and Logic '0' to be applied to the transistor closer to the output node in the PULL-DOWN side. Consider Ioff for PMOS and NMOS transistors as 20 nA, and 10 nA respectively.

a) 30 nA
b) 6.01 nA
c) 1.01 nA
d) 1.12 nA
e) 10 nA
f) 2.13 nA
g) 0.56 nA
h) 0.5 nA

6) Evaluate the subthreshold-leakage current for 2-NAND gate when the inputs of 1, and 0 are applied. Consider Logic '0' to be applied to transistor closer to ground rail, and Logic '1' to be applied to the transistor closer to the output node in the PULL-DOWN side. Consider Ioff for PMOS and NMOS transistors as 20 nA, and 10 nA respectively.

a) 30 nA
b) 6.01 nA
c) 1.01 nA
d) 10 nA
e) 5 nA
f) 2.13 nA
g) 0.56 nA

h) 0.5 nA

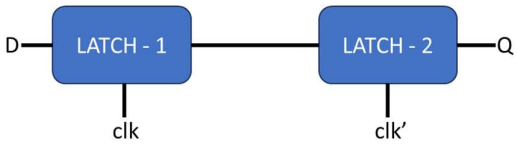
7) Determine the static power for 3-NAND gate for logic 011 where logic "0" is applied to the transistor closer to the output node in the PULL DOWN side. Consider Ioff for PMOS and NMOS transistors as 20 nA, and 10 nA respectively, with Igate-NMOS-leakage to be 8 nA.
   a) 10 nW
   b) 48 nW
   c) 26 nW
   d) 24 nW
   e) 56 nW
   f) 16 nW
   g) 20 nW
   h) 30 nW

8) Determine the static power for 3-NOR gate for logic 100 where logic "1" is applied to the transistor closer to the output node in the PULL UP side. Consider Ioff for PMOS and NMOS transistors as 20 nA, and 10 nA respectively, with Igate-NMOS-leakage to be 8 nA.
   a) 36 nW
   b) 38 nW
   c) 28 nW
   d) 10 nW
   e) 20 nW
   f) 25 nW
   g) 8 nW
   h) 30 nW

9) Select the correct statement.
   i. Stacking reduces subthreshold leakage.
   ii. Latch is an edge sensitive device.
   iii. Flip-flop is two back-to-back connected latches with clk and clk' connected their clock port.
   iv. Flip-flop is a edge sensitive device

   a) i
   b) ii, iii
   c) ii, iv
   d) iii
   e) i, ii, iii
   f) i, iii, iv
   g) i, ii, iv
   h) iv

10) The following is _____ .



a) negative edge triggered flip-flop
b) positive edge triggered flip-flop
c) positive level latch
d) negative edge latch
e) inverter-buffer
f) Jamb latch
g) Clocked CMOS (tristate inverter)
h) behaviour cannot be predicted

Solution:

1) **c) To avoid the Dynamic output**
   Conceptual

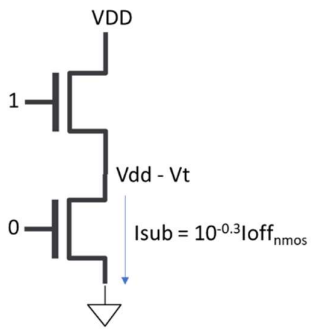
2) **g) 12**
   Conceptual

3) **c) 1.185W**
   $I_{sub\ logic} = 200 \times 10^6 \times 12 \times 0.025\mu m \times (0.95 \times 10nA/\mu m + 0.05 \times 100nA/\mu m) = 0.87A$
   $I_{sub\ memory} = 800 \times 10^6 \times 4 \times 0.025 \times 10 \times 10^{-9} = 0.8A$
   $I_{gate\ logic + memory} = 5nA/\mu m \times (200 \times 10^6 \times 12 + 800 \times 10^6 \times 4) \times 0.025\mu m = 0.7A$
   Pstatic = 1.185W

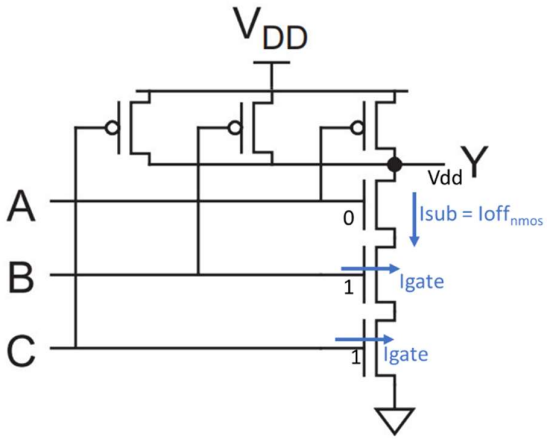
4) **e) 41.04W**
   $P_{switching} = \alpha C V_{dd}^2 f$
   $= (1.8fF/um) \times (0.1 \times 200 \times 10^6 \times 12 + 0.02 \times 800 \times 10^6 \times 4) \times 0.025 \times 3Ghz$
   $= 41.04W$

5) **e) 10nA**
   Ioff = Isub = 10nA

6) **e) 5nA**
   $I_{off} = I_{sub} \times 10^{-0.3} = 0.5011 \times 10nA = 5nA$

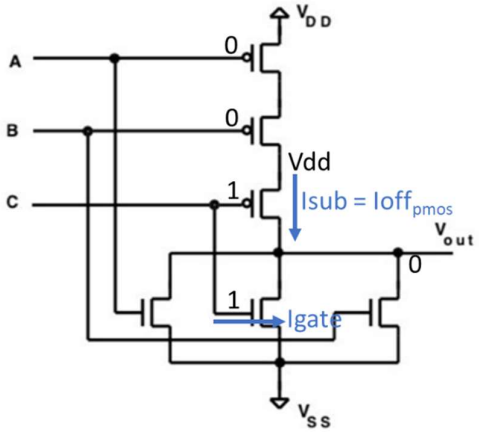


7) **c) 26nW**



Istatic = $Ioff_{nmos}$ + $2Igate_{nmos}$ = 10 + 8 + 8 = 26nA
Pstatic = 26nW

8) **c) 28nW**



Istatic = $Ioff_{pmos}$ + $Igate_{nmos}$ = 20nA + 8nA = 28nA
Pstatic = 28nW

9) **f) i, iii, iv**
Conceptual

10) **a) negative edge triggered flipflop**
Conceptual