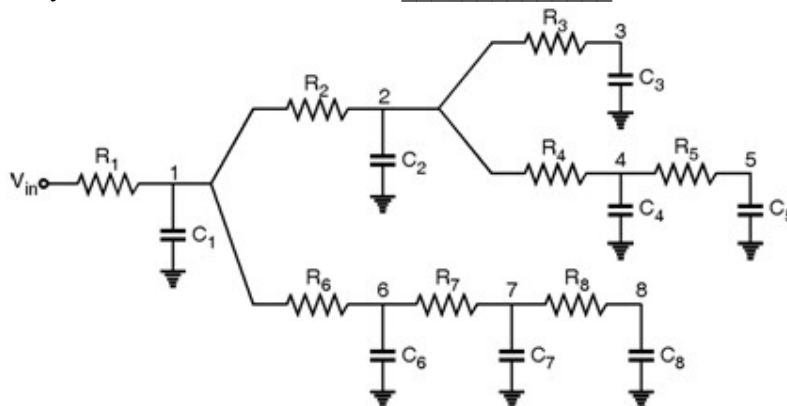


## Week - 4

- 1) The tpdf and tpdr of an N input NAND gate is
  - a)  $RC(N^2+5N)/2$ ,  $RCN(N+2)$
  - b)  $RC(2N^2+5N)/2$ ,  $RCN(N+2)$
  - c)  $RC(5N^2+5N)/2$ ,  $RCN(N-4)$
  - d)  $RC(3N^2+5N)/2$ ,  $RCN(N)$
  - e)  $RC(2N^2+2N)/2$ ,  $RCN(N-3)$
  - f)  $RC(2N^2+4N)/2$ ,  $RCN(N+7)$
  - g)  $RC(2N^2+N)/2$ ,  $RCN(N-9)$
  - h)  $RC(2N^2+6N)/2$ ,  $RCN(N-1)$
- 2) The tpdr and tpdf of an N input NOR gate is
  - a)  $RC(2N^2)$ ,  $RCN(2N+2)$
  - b)  $RC(3N^2+N)$ ,  $RCN(2N)$
  - c)  $RC(N^2+N)$ ,  $RCN(2N+3)$
  - d)  $RC(4N^2+5N)$ ,  $RCN(2N+4)$
  - e)  $RC(2N)$ ,  $RCN(N+3)$
  - f)  $RC(2N^2+3N)$ ,  $RCN(N+2)$
  - g)  $RC(2N^2+2N)$ ,  $RCN(N+1)$
  - h)  $RC(N^2+2N)$ ,  $RCN(2N+1)$
- 3) What is the logical effort for the input in a tristate based 2:1 multiplexer, considering long channel current model? Note that select lines are not inputs
  - a) 8
  - b) 1
  - c) 2
  - d) 16
  - e) 4/3
  - f) 5/3
  - g) 7/3
  - h) 10
- 4) For a 4-NAND (4 input NAND gate), what is the propagation delay falling and rising delay as per the ELMORE Delay method?
  - a) 16 RC & 16 RC
  - b) 10 RC & 10 RC
  - c) 24 RC & 24 RC
  - d) 17 RC & 17 RC
  - e) 18 RC & 24 RC
  - f) 17 RC & 16 RC
  - g) 16 RC & 16 RC
  - h) 10 RC & 10 RC

- 5) For a 4-NOR (4 input NOR gate), what is the propagation delay falling and rising delay as per the ELMORE Delay method?
- 16 RC & 16 RC
  - 10 RC & 10 RC
  - 24 RC & 24 RC
  - 17 RC & 17 RC
  - 36 RC & 24 RC
  - 17 RC & 16 RC
  - 16 RC & 16 RC
  - 13.4 RC & 17.6 RC
- 6) What is the logical effort of 4-NOR (4-input NOR) gate considering long channel current model?
- 2.51
  - 6.55
  - 3
  - 6
  - 2
  - 4
  - 8
  - 1
- 7) What is the logical effort of 4-NAND (4-input NAND) gate considering long channel current model?
- 1.59
  - 2.79
  - 3
  - 6
  - 2
  - 4
  - 8
  - 1

- 8) The elmore delay from node  $V_{in}$  to node 4 is \_\_\_\_\_ .



- a)  $R_1C_1 + R_1C_6 + R_1C_7 + R_1C_8 + (R_1 + R_2)(C_2 + C_3) + (R_1 + R_2 + R_4)(C_4 + C_5)$   
 b)  $R_1C_1 + R_2C_6 + R_1C_7 + R_1C_8 + (R_3 + R_2)(C_2 + C_3) + (R_1 + R_2 + R_4)(C_1 + C_5)$   
 c)  $R_1C_1 + R_2C_5 + R_1C_7 + R_1C_8 + (R_6 + R_2)(C_2 + C_3) + (R_1 + R_2 + R_4)(C_3 + C_5)$   
 d)  $R_1C_1 + R_2C_3 + R_1C_7 + R_1C_8 + (R_8 + R_2)(C_2 + C_3) + (R_1 + R_2 + R_4)(C_6 + C_5)$   
 e)  $R_4C_1 + R_4C_4 + R_1C_7 + R_1C_8 + (R_3 + R_2)(C_2 + C_3) + (R_1 + R_2 + R_4)(C_2 + C_5)$   
 f)  $R_4C_1 + R_4C_5 + R_1C_7 + R_1C_8 + (R_1 + R_2)(C_2 + C_3) + (R_1 + R_2 + R_4)(C_3 + C_5)$   
 g)  $R_4C_1 + R_4C_7 + R_1C_7 + R_1C_8 + (R_6 + R_2)(C_2 + C_3) + (R_1 + R_2 + R_4)(C_8 + C_5)$   
 h)  $R_4C_1 + R_4C_8 + R_1C_7 + R_1C_8 + (R_1 + R_7)(C_2 + C_3) + (R_1 + R_2 + R_4)(C_5 + C_5)$

9) According to ELMORE delay method, determine the propagation falling delay for 2-NOR gate which is sized to P:N as 4:1 ?

- a)  $8RC$   
 b)  $16RC$   
 c)  $24RC$   
 d)  $10RC$   
 e)  $72RC$   
 f)  $12RC$   
 g)  $3RC$   
 h)  $9RC$

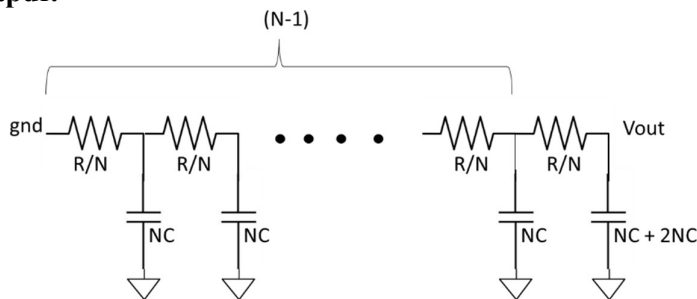
10) According to ELMORE delay, determine the propagation rising delay for 2-NAND gate which is sized to P:N as 2:2 ?

- a)  $8RC$   
 b)  $16RC$   
 c)  $24RC$   
 d)  $36RC$   
 e)  $72RC$   
 f)  $12RC$   
 g)  $3RC$   
 h)  $9RC$

### Solution:

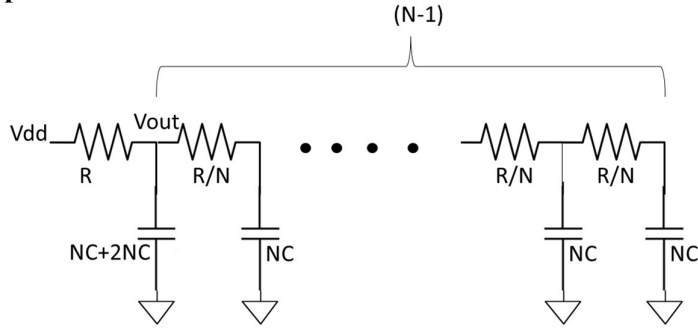
1) a)  $RC(N^2+5N)/2, RCN(N+2)$

**tpdf:**



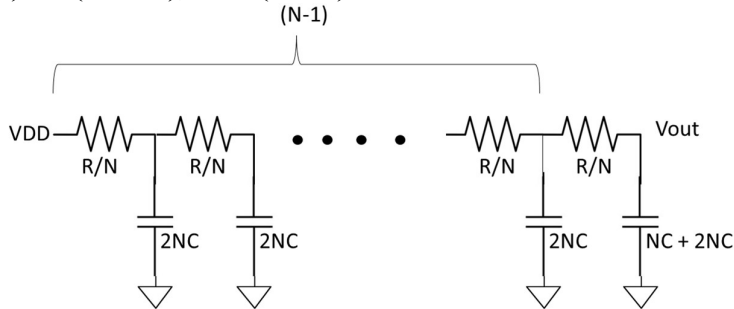
$$t_{pdf} = \frac{R}{N} \times NC + \frac{2R}{N} \times NC + \dots + \frac{(N-1)R}{N} \times NC + R \times 3NC = RC(N^2+5N)/2$$

**tpdr:**

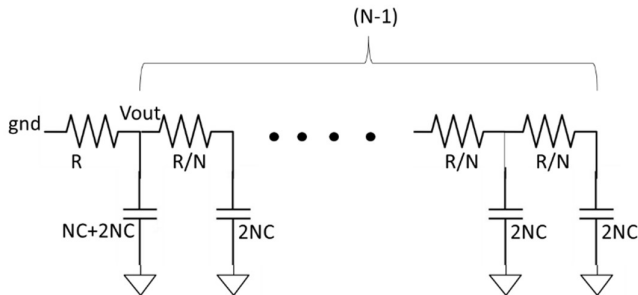


$$\mathbf{tpdf} = R \times 3NC + R \times NC \times (N - 1) = RCN(N+2)$$

2) **h)  $RC(N^2+2N)$ ,  $RCN(2N+1)$**



$$\mathbf{tpdr} = \frac{R}{N} \times 2NC + \frac{2R}{N} \times 2NC + \dots + \frac{(N-1)R}{N} \times 2NC + R \times 3NC = RC(N^2+2N)$$



$$\mathbf{tpdf} = R \times 3NC + R \times 2NC \times (N - 1) = RCN(2N+1)$$

3) **c) 2**

4) **e)  $18RC$  and  $24RC$**   
Formula based.

5) **e)  $36RC$  and  $24RC$**   
Formula based.

6) **c) 3**

$$g = (1+8)/3 = 3$$

7) **e) 2**

$$g = (2+4)/3 = 2$$

8) **a)  $R1C1 + R1C6 + R1C7 + R1C8 + (R1 + R2)(C2 + C3) + (R1 + R2 + R4)(C4 + C5)$**

Application of elmore delay model.

9) **d) 10RC**

4:1 2-NOR gate is a symmetric gate, with 2:1 inverter as the benchmark. So, direct application of formula.

10) **a) 8RC**

2:2 2NAND gate is a symmetric gate, with 2:1 inverter as the benchmark. So, direct application of formula.