MARK THOMAS DERBYSHIRE

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OBJECTIVE

RF-Hardware-Engineering position requiring detailed **RF/Analog**, High-Speed Digital (or Optical) and/or **MEMS** design at the system, board and/or chip level

EDUCATIONAL BACKGROUND

- Master of Science in Electrical Engineering/Minor in Mathematics, Washington State University (WSU), August 1993, Grade Point Average (GPA) 3.89 of 4.0, Master's program focused on Electro-Magnetics and Semiconductor Theory
- Bachelor of Science in Electrical Engineering, WSU December 1989, GPA 3.56 of 4.0, Cum Laude, Four "Presidential Honors" for high GPA
- **Two US patents**: 9,570,792 "RF Splitter/Combiner System and Method", 7,409,862 "Systems and Methods For Isolation of Torque and Sense Capacitors of a MEMS Accelerometer"
- **President/Owner of BBTLine, LLC** an RF Consulting and RF Product Development Corporation…www.bbt-line.com

WORK EXPERIENCE

Teradyne, Semiconductor Test Division, North Reading, Massachusetts, October 2011 to December 2016. 5+ year contract Designing/Simulating RF circuits (50 ohm single-ended and 100 ohm differential) to **85 GHz** for final incorporation into next generation "Zeta" microwave semiconductor test system and "Pegasus" proprietary 32.8 Gb/s serial data interface system. High-End TDR test equipment (7 ps risetime, Tektronix) and 50 GHz Keysight VNA used for measurements. Hardware Development and Simulations include: VCA design (VCA=voltage controlled attenuator, pi and tee configurations, M/A Com MA4SPS420 PIN diodes), M/A Com MASW-style SP4T PIN switches, 20 dB microstrip coupler design (15 dB directivity at 6 GHz), Peregrine switches/attenuators, Hittite HMC637 distributed amplifiers (closed-loop biasing), SMA, SMP and SMPM Connector Launch Optimizations (edge-launch and surface-launch style simulations with HFSS **.sat** models and measurements to **50 GHz**), Interposer simulations for Automotive Radar Applications (77 GHz), Via Transition optimization through very dense high layer count boards (36 layer), Optimized RF launches into and out of chip transitions (e.g., **HMC842, 848, 847, 958 chip family** used for 32.8 Gb/s system), Co-simulation of both SPICE-level broadband chip models (ADI Proprietary) with board-level HFSS models. High IP3 performance, low return loss, high isolation (150 dB), low insertion loss, minimum jitter, clean eye diagrams, minimal parasitics are the primary design goals. Eye diagrams and jitter analysis performed with ADS Transient simulator. Very tight Layout/Simulation coordination to ensure that the board layout folks preserved intended RF performance of design (initially set by simulations). System-level analysis of signal chains for Zeta and Marconi systems (Gain, IP3, NF). Mechanical Module housing isolation study (working with Mechanical Engineers, module housings and boards were prototyped and measured to ensure that module port-to-port RF isolation goals were met…using several styles of TennMax conductive gasketing, 150 dB isolation levels were achieved with triple rows of vias for CPWG). Member of design teams **Zeta** (**"FEM"** (Front-End Module) and **"SA"** (Splitter/Attenuator Module**)), Pegasus (32.8 Gb/s),** and **Marconi** systems**.** Worked with teams located in both North Reading, MA and Agoura Hills, CA. **RF Magnetics**: broadband ferrite combiner design utilizing material 61 and material 43 ferrite beads with 34 mil diameter conformable coax (CST simulations and board prototyping), broadband combiner prototype utilizing Mini-Circuits 4 GHz transformer. Intensive Electromagnetic EM simulation environment (HFSS, Momentum, CST) of numerous board-level circuits including multi-layer board via transitions and equalizer circuits (for flattening amplifier responses over 50 to 6000 MHz bandwidth); all simulations include component parasitics and board parasitics (with follow-on measurements to confirm simulation results). Extensive use of following EM simulators: Keysight **ADS2016.01, CST and Ansys HFSS version 17 (HFSS high performance computing on a Linux "computer farm"…accessing 60 machines simultaneously with TeraBytes of RAM for high via count, high isolation simulations, utilizing 3 Ansys HPC licenses**). Rogers 4350, Isola Astra MT, Isola Tachyon100G substrates utilized on 10 and 20 mil cores. Fast 2-layer prototype RF layouts generated using ADS Momentum (gerber files sent to either Advanced Circuits or AP Circuits for quick-turn boards). Numerous ADS circuit/Momentum optimizations. Detailed RF layout instructions provided to Teradyne layout personnel (Cadence Allegro tools and viewer utilized) by way of .dxf files and Word documents summarizing specific layout details and simulation results. DV (Design Verification) Testing of FEM and SA modules. Broadband (500 MHz to 6.5 GHz) Wilkinson splitter design in HFSS and "round-robin" comparison with CST and EMPro simulators (along with prototype splitter measurement verification of simulations performed in all three simulators). Very fluent with these high-end simulators: Ansys **HFSS (20 years experience), Keysight ADS (Momentum, Tran, HB)…20 years experience, CST, EMPro.**

Lumedyne Technologies, San Diego, CA, July 2010 to July 2011. Development of an optically-based MEMS accelerometer using a Fabry-Perot interferometer (an "etalon"). MEMS/Optical accelerometer concept was spun out of SPAWAR Naval Labs by Dr. Richard Waters. I was responsible for system-level modeling of closed and open loop systems (using Agilent ADS and Simulink software). Also developed test boards and test platforms for evaluating/characterizing the accelerometers. Investigated various VCSEL, RCLED, LED light sources. Modeled system noise contributions from photodiodes. Designed Receive-side electronic chain (TIA, ADC, analog divider circuitry, etc.) and Transmit-side electronics (laser-pulsing circuit, constant current source, etc). Developed Time to Digital Converter (TDC) evaluation boards for ACAM GP21 chip. **Agilent ADS** simulator and **National Ultisim/Multisim** layout/schematic package used extensively.

Raytheon, Tucson, AZ, August 2009 to July 2010. Responsible for internal Raytheon S-band (S-band = 2 to 4 GHz) receiver design for the SM-3 Missile. This receiver was a significant cost-saver over the existing Cobham design (this receiver material cost was approximately $400 versus the $10K Cobham design). Receiver implements FSK modulation…specifications are at the secret level, so not a lot of detail here. Rogers 4350B board material, interdigital filter design for image rejection (designed in ADS Momentum), SMA connector launch simulations/optimization using **Ansys HFSS**, 14 bit ADC (TI ADS6149), high order IF lumped bandpass filter design (ADS), PIN limiter circuit (AVX 0603 coupler + PIN diode) to limit front-end power to +10 dBm. Significant cost, weight, and power consumption reductions over existing external Cobham design. Factor of 25X in cost reduction over existing farmed-out receiver design. Ansys HFSS version 12 and **Agilent ADS2009** simulators used extensively.

Altierre Corporation, San Jose, CA, January 2009 to April 2009. Senior RF Engineer responsible for development of wireless radio in the ISM band (2.4 to 2.483 GHz). The Altierre wireless system is deployed in a grocery store (e.g., Safeway, Kroger); the system consists of an "Access Point" (AP), mounted at ceiling level in the center of the store, which communicates with thousands of "tags" located throughout the store (20 to 40

thousand for a large store).   The TDMA system uses 79 hopping channels (1 MHz channel spacing) with FSK modulation (250 KB/s data rate).   A "tag" is comprised of an Altierre proprietary transceiver chip, an LCD for displaying product details, and TX/RX dipole antennas.   The AP consists of digital and RF boards powered from POE (Power Over Ethernet).   The AP has one TX and two RX SMA connections (for connection to 7 dBi "whip" dipole antennas), one Cat-5 connection for POE/network, and one Cat-5 for "syncmaster" (for sync'ing up multiple AP's in larger stores). Responsible for re-design of the RF board to improve overall performance (sensitivity, power supply rejection, shielding, PCB layout), simulation of tag antenna far-field patterns using **CST-2009** Electromagnetic software, FCC certification of the AP.   TX section utilized the Skyworks SKY72300 dual synthesizer chip, RX section utilized Analog Devices ADF4154 Fractional-N synthesizer.   Final TX power output stage was two watts utilizing the Sirenza SZP-2026Z amplifier.   **PADS 2007** PCB Layout software used for re-layout of Access Point RF board.

Agilent Technologies, Everett WA, March 2007 to July 2008.   "Expert" RF Engineer responsible for design of a small/low-cost 20 MHz to 6 GHz spectrum analyzer geared towards outdoor/indoor Geo-Location and Spectrum Monitoring Applications.   Internal project name was "Minnow". In an urban environment, multiple units are synchronized (GPS time base) so that correlation algorithms can effectively lower the system noise floor and identify signal direction by TDOA (Time Difference of Arrival).   Responsible for all aspects of the RF hardware design: "inter-digital" RF band-pass filter design (simulations in ADS Momentum, prototype verification), schematic entry and board layout (**Altium Designer 6 software**), BOM generation, component selection, temperature/spurious/noise figure/IP3/spurs-with-input/residual testing.   Working with the Mechanical Engineer, I drove the design of the RF section of the mechanical enclosure for maximum isolation between RF stages (each critical stage in its own enclosure well with shielding cans and Gore surface-mount shielding strips).   Design incorporated six ninth order "inter-digital" filters on a Rogers 4350B substrate (εr=3.66, TanD=.004): five of the filters were used as "pre-selector" filters covering the range 1.7 to 6 GHz, the sixth filter was used to define the first IF bandwidth (2.1 GHz center, 100 MHz bandwidth, two in cascade).   Dense design: 1600 surface mount components on an 8-layer board (roughly the size of half a sheet of standard paper), 0402 components, 20 mil component spacing, and 5000 8-mil diameter blind vias on top/bottom board layers (for maximum RF isolation between stages). Design had three LO's utilizing the Analog Devices ADF4106 and ADF4360-2 PLL chips.   Two broadband Synergy VCO's (2 to 4 GHz) were utilized.   Final IF center frequency was 70 MHz with 20 MHz bandwidth (defined by two cascaded SAW filters), digitization at 56 MHz set by OCXO.   Also designed a ninth order 70 MHz filter to piggy-back on to the main RF board and replace the SAW's for applications where the SAW filter 100 ns group delay ripple was too high.   RF amplifiers consisted of multiple stages of Mini-Circuits "Gali" and ERA-6 style amplifiers, RFMD NLB-400, and Agilent MGA82563.   6 GHz Hittite SP8T switches and Skyworks SP2T switches were utilized.   M/A Com and Mini-Circuits 31 dB attenuators (1 dB step) were used to control system signal level, noise figure and IP3.   Digitization occurs using a Linear Technologies LTC2205 (14 bit A-to-D) with an LTC6400 pre-amplifier.   System noise figure ranged from 11 to 23 dB (depending upon attenuator settings) and IP3in ranged from -20 to +10 dBm.   12 watts total RF board power consumption, 24 watts total system power.   Simulations using ADS2006A, ADS Momentum, ADS EMDS (3-D simulator) occurred at all levels (i.e., LO phase noise, filter design, matching networks, NF/IP3 system budget, etc.).   Mini-Circuits mixers were used (ADE-42 and MCA1-60MH) for the primary RF down-conversion and an active mixer (Analog Devices AD8343) was used for the final IF down-conversion. There are essentially seven paths through the system: two "low-band" paths (20 MHz to 1.7 GHz) and five "high-band" paths (1.7 GHz to 6 GHz).   Agilent's high-end PSA's (Performance Spectrum Analyzer) were used extensively during all phases of system testing.

Honeywell DSES (Defense/Space Engineering Systems), Redmond WA, October 2002 to December 2006.   Principal Electrical Engineer responsible for design of commercial/military MEMS (Micro Electro-Mechanical Systems) accelerometer systems.   OPA ("Out of Plane Accelerometer") and IPA ("In Plane Accelerometer") MEMS capacitively-coupled silicon accelerometers were the focus.   Closed-loop servos and open-loop design architectures were explored.   The commercial effort required integrating a Microsensors MS3110 ASIC with the MEMS accelerometer at the hybrid level (wire-bonding in an LCC20 style surface mount package); target was a precision accelerometer for less than $100. The military effort utilized open/closed loop electronics with two 100-pin BGA ASIC's originally developed by Draper Laboratories [3rd order Delta-Sigma data conversion (DAC and ADC), AMI "C5" .5 um CMOS process, BGA-style packages, device-level modeling of the analog ASIC and DSP/VHDL modeling of the digital ASIC were performed with Agilent ADS software].   Military deployed these 3-axis "triax" accelerometer units in "IMU's" (Inertial Measurement Units) for JDAM (smart-bomb) and other Army "Common Guidance" high-g applications (up to 20 kg Howitzer shots).   Differential capacitance detection from the accelerometers was on the order of attoFarads (1e-18 Farads); 100 micro'g/√Hz performance. An LPKF Protomat 95S PCB milling machine was utilized extensively for prototyping printed circuit boards and developing test fixtures.   Protel DXP was used for single-axis test board schematic/layout entry.   Production three axis "triax" boards were developed in Mentor... 12 layer Rogers 4350 boards using blind/buried vias for dense routing of BGA packages.   All aspects of the Agilent ADS simulator were utilized (RF/Analog/DSP co-simulations, VHDL co-simulation, Harmonic Balance, Transient, BSIM3 nonlinear FET model, etc.) for system-level and FET-level simulations of the accelerometer system.   HPA1 ("High Performance Accelerometer") was the acronym for the Analog ASIC, HPAD ("High Performance Accelerometer, Digital") was the acronym for the DSP chip used to process HPA1 signals.   Stages in the HPAD chip included down-conversion, CIC filtering, Butterworth filtering, PI controller, square root function, and Sigma-Delta DAC.   Next generation HPA2/HPAD2 ASIC's currently (2005) being developed...HPA2 in a Cadence IC5.1.41/ADS2005A circuit simulator environment, in the AMI C5 CMOS process, as a joint Honeywell/Draper Laboratories effort.   Experienced with UnHoltz-Dickie vibration table for measurement of accelerometer VRE (Vibration Rectification Error) performance...VRE is the non-linear performance of an accelerometer typically measured in micro-g per g-squared.   Typical performance goal of the accelerometers tested was 100 ug/g^2.   Invention Disclosure: "Isolated Torque and Sense Mechanism" which outlines an accelerometer with two anodic bonds for separating the torque and sense capacitors and reducing torque signal injection into the trans-impedance amplifier.

Terabeam Corporation, Redmond WA, July 2000 to July 2002.   Senior RF Engineer in the FSO (Free Space Optics) field.   Responsible for design of optical transmitters/receivers ranging in data rates from 125 Mb/s to 2.5 Gb/s.   Data   channel receivers utilized InGaAs (Indium Gallium Arsenide) and silicon APD's (Avalanche Photo Diodes) with sensitivities in the range of -48 dBm for 125 Mb/s data and -38 dBm for 1.25 Gb/s data (optical power levels).   APD receivers required high voltage circuit design with temperature compensation.   Another low frequency receiver design utilized a germanium "quad" cell for purposes of tracking and alignment of the system optical transceiver heads; this design utilized an extremely low noise amplifier chain with AGC (Automatic Gain Control).   Transmitter designs utilized Fujitsu/Agere DFB (Distributed Feedback) lasers in butterfly package feeding an EDFA (Erbium Doped Fiber Amplifier) amplifier.   Filed a patent application entitled "Switched Optical Detector Tracking For Wireless Optical Communication Systems".   Agilent 86130A BERT (Bit Error Rate Tester) and Agilent 86100A [sampling scope with O/E (Optical/Electrical) and differential TDR (Time Domain Reflectometer) sub-modules] formed the heart of my test bench along with Agilent

spectrum analyzer and network analyzer.   Agilent ADS (Advanced Design System) simulation software was utilized throughout employment with Terabeam.

Vixel Corporation, Bothell, WA, May 1999 to June 2000.   Principal RF Engineer responsible for next generation (2.5 Gigabit/s data rate, 100 picosecond rise/fall times) fiber optic transceiver development utilizing VCSEL (Vertical Cavity Surface Emitting Laser – multimode, 850 nm wavelength) transmitter, high frequency optoelectronic PIN diode receiver assemblies, 2.5 Gb/s GaAs Serializer/Deserializer chips.   Project involves extensive use of the following software/hardware tools: Agilent ADS software, high frequency SPICE simulations, PADS schematic/PCB layout software, Hewlett Packard 3.2 Gigabit/s jitter analysis system including BERT (Bit Error Rate Tester), Agilent 83480 high speed sampling scope (20 GHz front end bandwidth) with 83487A 2.8 GHz optical/electrical converter plug-in and HP54751A TDR plug-in, Advantest optical power meter, JDS Fitel optical attenuator.   Eye diagram analysis, BER analysis (10e-12 BER goal), jitter analysis are the mainstay performance indicators.

Also, high speed (3.2 Gb/s, 100 picosecond rise/fall times)) backplane design for high port-count Fibre Channel switch.   Backplane design requires: 1) extensive modeling of vias, couplers, connectors, transmission line geometries with HFSS (High Frequency Structure Simulator) software from both Ansoft (version 7.0) and Agilent (version 5.5), 2) high frequency SPICE-like simulations (using Agilent ADS software), and 3) evaluation of high speed connectors from Teradyne (VHDM and HSD), AMP (HS3), Siemens (SpeedPac), FCI/Berg (Metral).

Metawave Communications Corporation, Redmond, WA, September 1997 to April 1999.   Principal RF Engineer involved with "skunkworks" GSM Smart Antenna system effort.   Project included travel to the U.K. for training/consulting time with a GSM organization called MAC (Multiple Access Communications, Southampton).   Responsible for system (RX and TX) RF Hardware development including the following:

a)   RX side RF switch matrix (four RF inputs and 12 RF outputs) with drop-in, all surface-mount RF components (M/A Com LNA's, Alpha splitters/digital attenuators/GaAs switches)   for operation in either the EGSM, DCS-1800, or PCS-1900 frequency bands.   Design included the following: an Altera EPF10K20 programmable logic device for control of all switching functions in accordance with the GSM TDMA format, a pilot tone and RF detector circuitry for path integrity checks, digital attenuators on all RF paths for path gain balance to within 0.5 dB.   The entire receive side noise figure, gain, and intercept point were set by this design.   12 layer FR-4 PCB.
b)   "uplink" scan receiver (essentially a "narrowband, IF-digitized" digital receiver) with drop-in RF components for all three frequency bands mentioned above.   The receiver chain consists of a single down-convert to a 200 kHz BW SAW filter center frequency of 199 MHz and then into a high speed A-to-D converter (Analog Devices AD6600, encode rate = 13MHz).   After the AD6600 was an Analog Devices "decimating receiver" (AD6620).   The AD6620 contains a numerically controlled oscillator, which performs a second down-conversion, and then three stages of digital filtering at base-band for extreme rejection of GSM "blocker" signals.   The design also included PLL design centered around the National Semiconductor LMX2320 synthesizer chip and a M/A Com VCO for good phase noise performance.   8 layer FR-4 construction.   ETSI GSM 5.05 specification guiding design.
c)   "downlink" scan receiver design for monitoring communications from the TX ports of the GSM base station transceivers.   Essentially the design mimics a mobile phone by utilizing half of the Analog Devices GSM chip set (ADmsp415 chip set).   Design included the National Semiconductor LMX2331A dual synthesizer chip, Analog Devices AD6459 IF subsystem chip (mixer, amplifier, I and Q demodulators, etc.), and an Analog Devices AD6421 chip (half of the ADmsp415 chip set).   This design provided GSM timing and control channel information to the "downlink processor board" of our system.
d)   TX combiner board.   This board's function is to combine four 40 watt RF signals (925-960 MHz) from GSM base station TX ports.   Very simple from a schematic standpoint but more difficult from a heat dissipation and mechanical standpoint.   The board utilized Anaren 3 dB Xingers and 6 dB couplers, RF Power Components, Inc. 100 watt and 150 watt "waste" loads, Rogers 4350 low loss dielectric substrate, AMP 2mm Hard Metric style backplane connectors and a massive heat sink (approximately 10" by 16" for heat dissipation from the "waste" loads.   Single layer microstrip construction.   Worked with Mechanical Engineers to define heatsink.
e)   TX side switch matrix and high power attenuator project (925 to 960 MHz).   This design built upon previously developed prototypes and utilized two versions of M/A Com high power PIN diodes for transmission/attenuation of up to 40 watt RF signals.   The design consisted of two SP5T (single pole five throw) switches and two high power attenuators (DAC voltage control), controlled by an Altera EPM7256A programmable logic device.   The SP5T's were very frequency sensitive, requiring λ/2 and λ/4 sections and judiciously placed tuning stubs for tuning out diode and other surface mount component parasitics.   Design also required a switching power supply, centered around Linear Technologies "ultra-quiet" LT1533 chip, to go from +24 VDC to -75 VDC for high reverse bias of PIN diodes.   Measurements were made on a prototype, RF modeling was performed using Ansoft Serenade software and schematic entry was completed.   Layout for this design was to begin in April.

Metawave Communications Corporation, Redmond, WA, June 1995 to September 1997.   RF Engineer developing Metawave's "Spotlight" Analog Smart Antenna product for the AMPS/NAMPS cellular bands.   Designs included the following:

a)   receive-side RF switch matrix (12 RF in's/16 RF out's, 824-849 MHz).   Several splitter/LNA/attenuator/GaAs switch sections to preserve system noise figure, gain, and IP3 of the entire RX RF chain of the "Spotlight" Smart Antenna product.   12 layer FR-4 PCB.
b)   transmit-side RF switch matrix (869-894 MHz).   Three stages of M/A Com RF digital attenuators on each path for accurate control of transmit side power levels.   12 layer FR-4 construction.   1 watt input levels.   12 RF in's and 16 RF out's.   Berg style RF connectors.
c)   AMPS/NAMPS RF "scan" receiver 824-849 MHz, dual down-conversion design consisting of Triquint front end LNA/mixer, Philips SA625 IF subsystem chip, TOKO SAW filter at IF, and Philips SA7025 fractional-N synthesizer.   Met IS-95 specifications for RF performance (adjacent/alternate channel rejection performance, intermodulation performance, sensitivity performance, etc.).   < 2ms RSSI scanning capability.

System Test Engineer for International Sensor Technology, Pullman, WA, February 1994 to June 1995: small, family-owned business originating from PhD's Laser-Heated Thermoluminescent Dosimetery (LHTLD) patent; Naval contract to deliver ship and shore radiation badge "readers":
  a)   The system used SYNRAD CO_2 lasers to locally heat an irradiated phosphor (personnel dosimeter); the heated phosphor would emit photons with photon density proportional to the radiation level; a high voltage photomultiplier tube gathered the photons and translated them into electronic pulses for dosimeter dosage measurement

b)   I was responsible for electronic debug, calibration, troubleshooting, and accuracy testing of both ship and shore systems

Research/Teaching Assistant for Washington State University, Pullman, WA, August 1991 to May 1993
a)   This position required grading course-work/exams, supervising laboratory experiments, giving course lectures, research in non-linear MOSFET characteristics, one-on-one tutoring of students in courses covering Electromagnetics, Control Theory, Digital circuits.   The position was with the Electrical Engineering Department and covered educational costs associated with my Master's degree as well as providing a salary.

Electrical Engineer for Naval Undersea Warfare Engineering Station (NUWES), Bangor, WA, February 1990 to August 1991
a)   Worked in the Acoustics Division of NUWES for first year.   Lead Engineer on the Noise Reduction System 4 (NRS4) which was responsible for gathering torpedo acoustic signatures.   The system incorporated "hydrophones" (underwater transducers) and all of the on-ship electronics to record torpedo acoustic data.   Responsibilities included system calibration, recording torpedo "shots" on the Dabob range and the Canadian Quinault range, troubleshooting, system and system documentation upkeep
b)   Worked in the Heavy Weapons Division for last six months.   Duties included Torpedo cable manufacture, cable repair, cable damage investigation, and automated cable test set development.
c)   Started at GS-7 ranking and obtained GS-11 ranking within 1.5 years.   Duties required "Secret" security clearance level

Summer Internship with the Boeing Electronics Company (BECO), summer 1988
a)   Assisted Senior Engineers with various projects, incorporated schematic revisions, put together project instructions to be issued to technicians, estimated cost of materials for two fairly large projects, monitoring of transformer current and voltage levels throughout Boeing complex, put together plans for installation of 60 Hz power.

TEST EQUIPMENT UTILIZED
Anritsu 3.2 Gb/s BERT (Bit Error Rate Tester), HP 3.2 Gb/s Jitter Analysis system, HP8510/HP8753E/HP8714 vector network analyzers, Rohde & Schwarz **FSEB20** spectrum analyzer with low phase noise option and vector analysis option (for demodulation of GMSK signal, eye diagrams, constellations, etc.), **HPE4419B** dual power meter, HP frequency and modulation domain analyzer for testing PLL step response, **HP8595E** spectrum analyzer with noise figure/phase noise personality cards, **HP8644B** ultra pure signal generator (phase noise = -136 dBc/Hz @ 20 kHz offset, used for GSM "blocker" testing of "uplink" receiver), **Fluke 6060 and HP8657B** series signal generators, 20 GHz Tektronix TDR (Time Domain Reflectometer), **HP8921/IFR** communications test sets (for AMP/NAMPS receiver performance measurements), HP portable Logic Analyzer for PLD troubleshooting, **HP4194A Impedance/Gain-Phase Analyzer**, **Agilent 83480** high speed sampling scope (20 GHz front end bandwidth) with **83487A 2.8 GHz optical/electrical converter** plug-in and **HP54751A Differential TDR** plug-in.

SOFTWARE TOOLS UTILIZED
Keysight ADS2016.01, Ansys HFSS 17, CST-2014 Electromagnetic Simulator (Time and Frequency Domain Versions), EMPro 2015.01, PADS 2007, Altium Designer, Cadence IC5141 (Virtuoso/Spectre for ASIC development), Ansoft Serenade version 7.5 (full linear and nonlinear RF analysis), **Ansoft Q3D Extractor** (for 3-D modeling of accelerometer capacitance), **Agilent ADS (with "Momentum" Planar Field Solver and DSP/RF/VHDL cosimulation)**, **Agilent HFSS (version 5.5)**, **HP Series IV Omnisys** (for system level RF gain, noise figure, and IP3 budgets), **MMICAD** linear RF simulator, **MATLAB**, **Protel '99** for schematic entry and PCB layout, **Orcad** schematic entry, **PADS** schematic/layout, **EZNEC** antenna analysis (Method Of Moments) software, **Microsim PSPICE** for digital simulations and low frequency VCO design, **Altera MAX+II design tools** for PLD (Programmable Logic Device) design, **Protel DXP**, **OrCad** Schematic Entry, **National Ultisim/Multisim** layout/schematic entry.

EDUCATIONAL/TRAINING COURSES/TRADE SHOWS ATTENDED WHILE ON THE JOB
Cadence IC5141/Virtuoso/Spectre 4-day training course (San Jose, May 2005), **"ADS Communications System Designer" Course** (9/2004, 3-day course, $\pi/4$ DQPSK receiver/transmitter development, DSP/RF cosimulation)**, Mentor XTK (**printed circuit board crosstalk analysis**), Matlab Simulink 4 day course, CTIA trade show, DesignCon 2000, Ansoft Eminence HFSS** 4 day training course; **Ansoft Serenade version 8.0** training course; **HP Series IV Omnisys** (RF systems analysis) 4 day training course; **Les Besser RF Techniques II**; 5 day **GSM training course\consultation** held in South Hampton, England.

MASTER'S PROJECT
Used experimental data to solve for the electric/magnetic constitutive parameters of many materials including a sample of carbon-fiber impregnated material used on the Boeing 777 aircraft.   The project required the use of a HP 8510 network analyzer in the X-band and iterative Newton-Raphson techniques to solve for the variables of the "reflection/transmission" technique found in the literature.

OTHER SALIENT COURSEWORK
a)   Modeling of electron velocity and electron scattering processes in GaAs.   The GaAs model assumed   multiple valleys (E-k plot) and covered inter- and intra-valley scattering processes involving phonon/photon and other particle collision effects.   Fortran coding required sparse matrix techniques, tri-diagonal solvers, scattering process PDF characterization, Monte Carlo simulation and a CRAY computer account.   Velocity vs. E-field results from the model closely matched literature results.
b)   charge transport in silicon – model required discretizing continuity equation, Poisson's equation, and other differential equations on a "mesh"; used Fortran language and sparse matrix techniques.
c)   Attended every Electromagnetics courses which WSU had to offer.   Topics covered include: diffraction mathematics, microwave/atmospheric propagation, waveguide analysis, optics (holography and 2D spatial Fourier transforms), fiber-optic mode solutions, Near/Far field antenna analysis, solving for diffraction fields from knife-edge, solving for radar cross sections of canonical geometries, use of iterative techniques for solving electromagnetic problems, complex variable mapping.
d)   VLSI Course – VLSI chip design (2 μm process, 1989) using Mentor Graphics software, SPICE modeling, and very dense D Flip-Flop architecture.   VLSI chip function was "pattern-recognition" of a digital vector.
e)   Microwave amplifier and filter design designed with Touchstone and microstrip; hands-on in WSU's Microwave laboratory.

f) Fabricated simple Schottky diodes in WSU's "clean" room as part of graduate-level semiconductor course.