DELPHI ENGINEERING GROUP

DATASHEET

ClkSync

Wideband Clock and Trigger Distribution System

The CLKSYNC is a clock and trigger distribution system that provides multiple, independent copies of clock and trigger signals for multi-channel, Giga-sample ADC and DAC boards. Up to twelve independent ADC or DAC clocks and triggers are synchronized.

The CLKSYNC offers a number of clock source options including: external clock, external reference and an internal clock with a low-noise 1ppm reference . Each of these clock sources can generate output signals in the range of 500 MHz to 3 GHz with jitter of less than 100 fs. Users can adjust the phase for each clock output.

Twelve individually adjustable trigger outputs are provided in the CLKSYNC. The rising edge of a positive external trigger signal is captured at a user-defined threshold. The delay of each output signal can be independently set from 0 to 6 ns, with 16 ps resolution. All trigger signals are synchronized with the selected main clock. The CLKSYNC also provides the user with a manual trigger.

The CLKSYNC is housed in a standard 1U chassis and can be used in desktop or 19" rack mount configurations.

BENEFITS

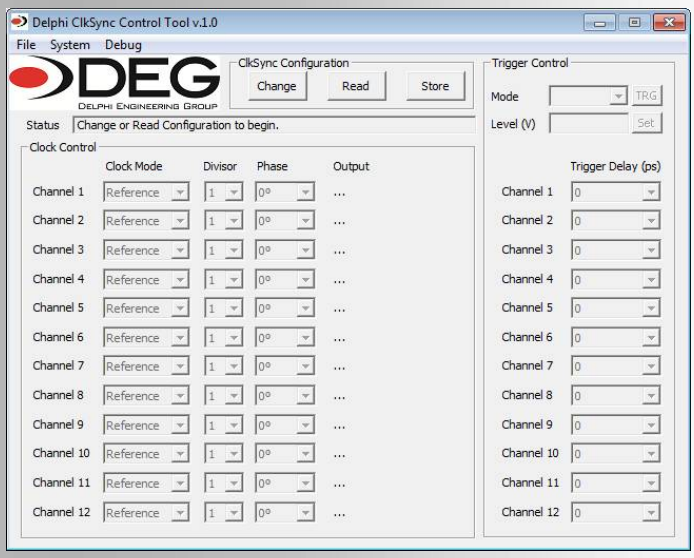
- Multi-Chassis Scalability
- Twelve Phase Matched Triggers
- Twelve Phase Matched Clocks
- Low Jitter and Phase Noise
- User Selectable Clocking Options: Main Clock, Divided Clock and Reference Clock

FEATURES

- Frequency Range: 500MHz to 3.0GHz
- External and Internal Clocking Options
- Desktop and 1U Rack mount Options
- Programmable User interface

PERFORMANCE

- Clock Jitter less than 100fs @ 3GHz
- Clock Frequency Divided By: 1,2,4,8,16
- Trigger Delay: 0 to 6ns, 13ps Step per Channel
- Clock Phase Adjustment: 360°, 64 Steps per Channel

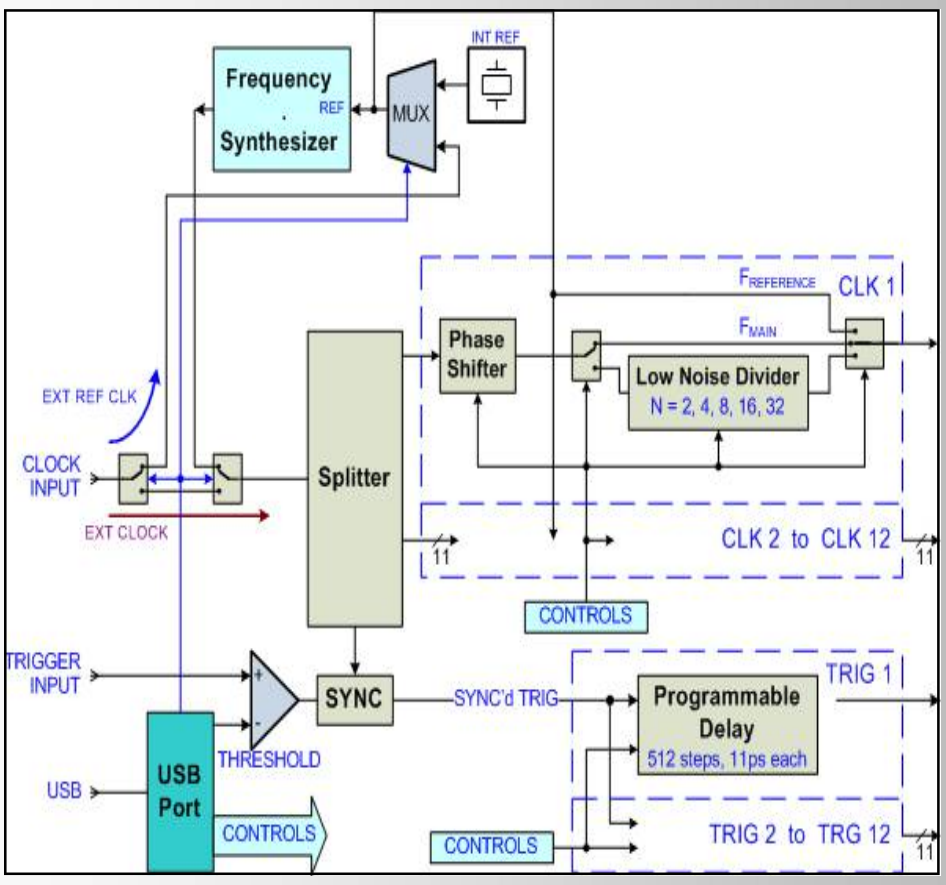


A USB controlled Windows GUI provides visualization of the ClkSync's configuration settings.

ClkSync Performance Specification

External & Ref Clock Input	Parameter
Amplitude	0dBm to 10dBm
Internal Reference Clock	1ppm Over Temperature Range
External Reference Clock	10MHz to 100MHz
Bandwidth: External Clock	500 - 3000 MHz
Bandwidth: Internal Clock	500 - 3000 MHz
Output Frequency Divided By	1,2, 4, 8, 16

Trigger Input	Parameter
Connectors	SMA Front Panel
Pulse	Positive Edge
Amplitude	0.1V to 1.25V
Rise Time	Less than 10ns. Sub-nanosecond edge recommended
Duration	5ns to 100us



ClkSync Block Diagram

About DEG

Delphi Engineering Group (DEG) provides a full range of high-performance COTS-based and customized digital receiver technology, products, and services for mission-critical applications in the aerospace, defense, and communications industries.