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Method for Troubleshooting Power Integrity Problems in Programmable Logic Device Electronic Systems by Embedded Measurement of Power Distribution Impedance

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Abstract

Power distribution networks (PDN) may degrade in time due to various reliability factors including tantalum capacitors with burned internal fuses that become open circuits, dried electrolytic capacitors, decoupling capacitors or interconnect solder joints open or with increased resistance. This paper proposes a method for troubleshooting power integrity problems in systems using programmable logic devices (PLD). The method configures part of the PLD to internally measure the impedance of its power distribution network. This embedded PDN measurement core uses only logic blocks commonly available in any existing PLD without the need of built-in dedicated circuits. The frequency profile of PDN impedance can be measured on production floors or remotely in systems installed in the field by activating and communicating with the embedded PDN impedance measurement core. Archived frequency profiles along various periods of time can help identify PDN issues or study any potential long-term power distribution degradation of systems.

Author Biography

Dr. Cosmin Iorga is the founder of NoiseCoupling.com and has accumulated over 20 years of experience in high-speed circuit design and troubleshooting at system, board, and integrated circuit levels, with emphasis on signal integrity, power integrity, and noise coupling reduction. Cosmin has earned his Ph.D. in electrical engineering from Stanford University, and he has filed more than 15 patents with 9 granted so far, covering innovative solutions in noise coupling reduction and signal integrity. Cosmin is the author of the book “Noise Coupling in Integrated Circuits: A Practical Approach to Analysis, Modeling, and Suppression”.

1. Introduction

Degradation or failure of power distribution networks (PDN) may have significant effects on functionality and performance of electronic systems. In programmable logic devices (PLD), PDN degradation may generate timing failures [1]. At the design stage of product development a lot of effort is made to develop low impedance power distribution networks. While the PDN impedance may meet requirements at product release stage, later over the product life various failure mechanisms may degrade the PDN performance. Time degradation of decoupling capacitors has been reported in [2], more specific analysis of time degradation of tantalum capacitors has been reported in [3], time degradation of aluminum capacitors has been reported in [4], and time degradation of leakage in capacitors has been reported in [5]. While total failure of PDN translates directly into system failure, which is easy to detect, partial degradation of PDN typically affect only the performance of systems [6] in ways that are sometimes hard to detect. Because PDN often provide redundancy in possible current flow paths and parallel configuration of multiple decoupling capacitors, detection and troubleshooting of partial failures of PDN components is often a difficult task.

Most common PDN failure mechanisms can be categorized into reduced decoupling capacitance, increased series resistance, open solder joints or interconnects that divert current flow increasing loop inductance, and high leakage paths or shorts between voltage rails.

Reduced decoupling capacitance may result from failure of only part of decoupling capacitors on a power supply rail. Since in this case there are still remaining functional decoupling capacitors, the result is a reduction of the overall decoupling capacitance. Additional effects result from changing the flow of transient currents, which now will find alternate flowing paths that result in increased loop inductance. Typical causes for decoupling capacitor failures depend on types of capacitors. For example tantalum capacitors tend to develop shorts through the dielectric which would then short the supply rails. Reliability studies of tantalum capacitors have been reported in [7], [8], and [9]. To avoid shorting the supply rails, manufacturers insert series fuses in tantalum capacitors, thus dielectric shorts translate into open-circuit capacitors. Ceramic capacitors may become open-circuit or may only reduce the capacitance value due to physical cracks in the dielectric. These cracks may be caused by mechanical or thermal stress. Failure analysis of ceramic capacitors has been reported in [10], miniaturized ceramic capacitors in [11], leakage in [12], high-temperature in [13], and electrode melting in[14]. Surface mount capacitors may become open or may develop high series resistance from malfunctioning solder joints. In aluminum capacitors ESR impedance increases due to polymer degradation, and electrolytic capacitors increase the ESR due to electrolyte loss. Normal aging of dielectric material may also lower the capacitance of some ceramic type capacitors.

Conductive paths of chip-to-package and package-to-PCB PDN interfaces may increase series resistance or may even become open due to electromigration, mechanical tension, or thermal stress. Degradation at PCB level has been reported in [15] and for blind vias in [16]. Degradation of series resistance and opens in solder joints and has been reported in [17], electromigration of BGA ball interconnects in [18], flip-chip solder bumps in [19], and die bond wires in [20].

These failure mechanisms may either make the entire PDN not functional or may only degrade the PDN performance. At system level circuits see this performance degradation as increased PDN impedance at certain frequencies or frequency ranges. Existing resonance peaks may shift in frequency and additional resonance peaks may appear. The increase in PDN

impedance increases the noise on power supplies, and new or frequency shifted PDN resonance peaks may now coincide with chip operational frequencies generating significant supply noise. At system level PDN degradation may result in functionality failures or performance issues that often may have an intermittent occurrence. Troubleshooting these types of PDN failure mechanisms needs to be able to evaluate the PDN impedance and to detect the frequency location and magnitude of resonance peaks. These problems and especially open circuit capacitors, open vias or solder joints, and increased series resistance are in general hard to identify using common test instruments due to redundant/parallel current paths and multiple decoupling capacitors connected in parallel.

2. Overview of the Proposed PDN Troubleshooting Method

This paper presents a method for troubleshooting power distribution network (PDN) problems in programmable logic devices (PLD) electronic systems by measuring on-die the electrical impedance of the power distribution network as seen by the PLD internal circuits. The measurement system is implemented in the programmable logic device by configuring and using only general configurable logic blocks and/or input-output blocks commonly available in any existing programmable logic device. All measurements are done inside the programmable logic device without the need of external test instruments.

The main advantage of using resources that are not specifically built-in for power distribution measurements is that this method can be used with most of the existing programmable logic devices (PLD) available on the market, including field programmable gate arrays (FPGA) and complex programmable logic devices (CPLD).

Another advantage of using resources that are not specifically built-in for power distribution measurements is that this method can be implemented in a programmable logic device temporarily only for characterization or troubleshooting purposes, after which the programmable logic device can be reconfigured back to the original functionality. This way, after characterization or troubleshooting, the programmable logic device resources used for power distribution impedance measurements are freed up and re-configured to perform other logic functions, saving cost and reducing power consumption.

A third advantage of using only internal resources of the programmable logic device is that this method can be used to remotely troubleshoot existing electronic systems that use programmable logic devices and operate in hardly accessible locations, like data communication equipment installed in the field. For example a common failure mechanism in electronic systems is internal shorting of tantalum electrolytic capacitors, which burns internal fuses built-in inside these capacitors intentionally by manufacturers. As a direct consequence, a burned capacitor becomes an open circuit and does not perform the intended power distribution decoupling function. Typical power distribution networks comprise multiple tantalum decoupling capacitors connected in parallel, and if some of them burn their internal fuses, the impedance of the power distribution increase. One way to detect an increase of power distribution impedance is to measure it; however, most existing techniques require major disruption of the electronic system to get access to measurement nodes and connect measurement instruments. The proposed technique allows more convenient troubleshooting by remotely accessing the programmable logic device and measuring the power distribution impedance. After troubleshooting, the programmable logic device can be reconfigured remotely back to the original functionality.

3. Description of the Proposed PDN Troubleshooting Method

This paper proposes a method for troubleshooting power integrity problems in systems using programmable logic devices (PLD) such as field programmable gate arrays (FPGA) or complex programmable logic devices (CPLD) by using embedded measurement of power distribution impedance.

The embedded measurement system is implemented inside a programmable logic device by configuring and using only logic blocks resources commonly available in any existing PLD, without using any built-in dedicated circuits, thus making possible the implementation of this method to programmable logic devices already used in existing electronic systems. All measurements are done inside the PLD without the need of external instruments, thus enabling the application of this method to systems operating in the field or in hard accessible areas.

The method measures the impedance of the power distribution network by using AC steady-state analysis. The AC steady-state analysis is implemented by applying a test AC current source to a power distribution network port (two terminals), thus injecting an AC current into the network, and measuring the resulting AC voltage on that network port. Figure 1 illustrates the application of this method to a system consisting of a die placed in a package, which is mounted on a printed circuit board (PCB). The power distribution network connects the voltage regulator module (VRM) to the circuits on the die and provides supply voltages decoupling through capacitors on the die, package, and PCB. The AC current source is represented by I_TEST and the measured AC voltage is represented by V_MEAS. The impedance is then calculated as the measured voltage divided by the injected current.

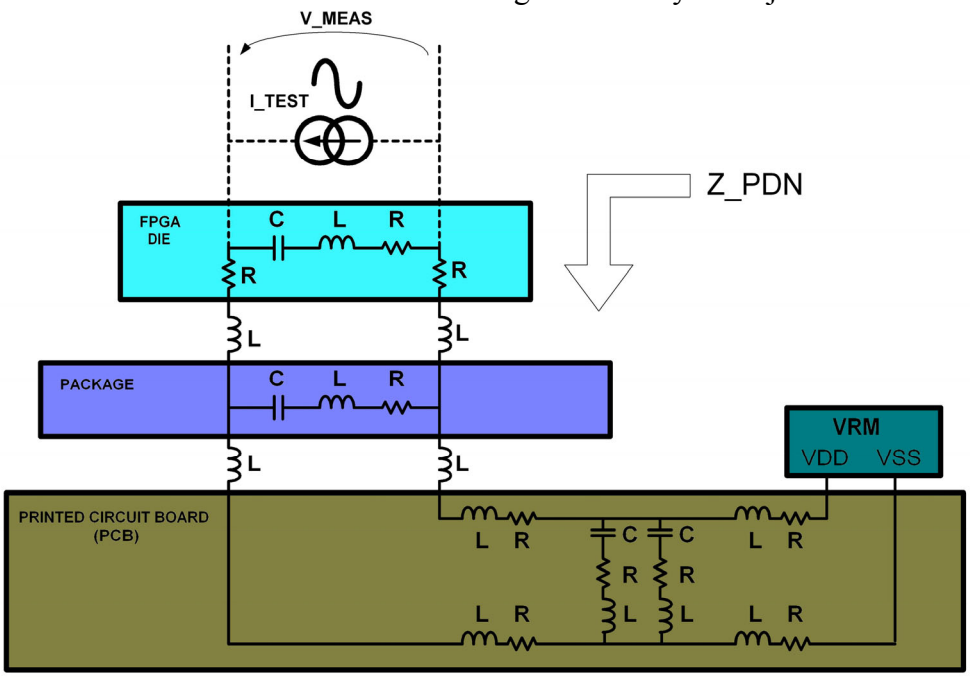

Figure 1. Example application of the proposed PDN troubleshooting method to a system consisting of a die mounted in a package and placed on a printed circuit board

AC steady-state analysis is largely applied in circuit calculations and simulations and uses linearized models of devices, thus the value of the injected current does not affect the measured impedance. However, when implementing this method to physical circuits we need to make sure that the injected current is sufficiently small so that it does not affect significantly the operating point of non-linear devices. This way PLD circuits still operate within the small-signal approximation, which is a fundamental condition of the AC steady-state analysis method.

In order to use the AC steady-state analysis impedance measurement method in PLD applications, we need to apply an AC current source to the power distribution network and we also need to measure the resulting AC voltage on the power distribution network. Both the AC current source and the AC voltage measurement have to be implemented in the PLD die. While there may be possible to design specialized circuits when PLDs are fabricated, these specialized circuits are not so convenient to implement since they may occupy significant area of the die, taking space from the overall number of configurable logic blocks of the PLD and increasing cost. To be applicable to existing PLD devices, the proposed method uses only common logic blocks available in any PLD device. To better understand this method let's look at an application example in a field programmable gate array (FPGA) type of PLD device.

Figure 2 shows a block diagram of a power distribution measurement system implemented in an FPGA by configuring only commonly available logic blocks.

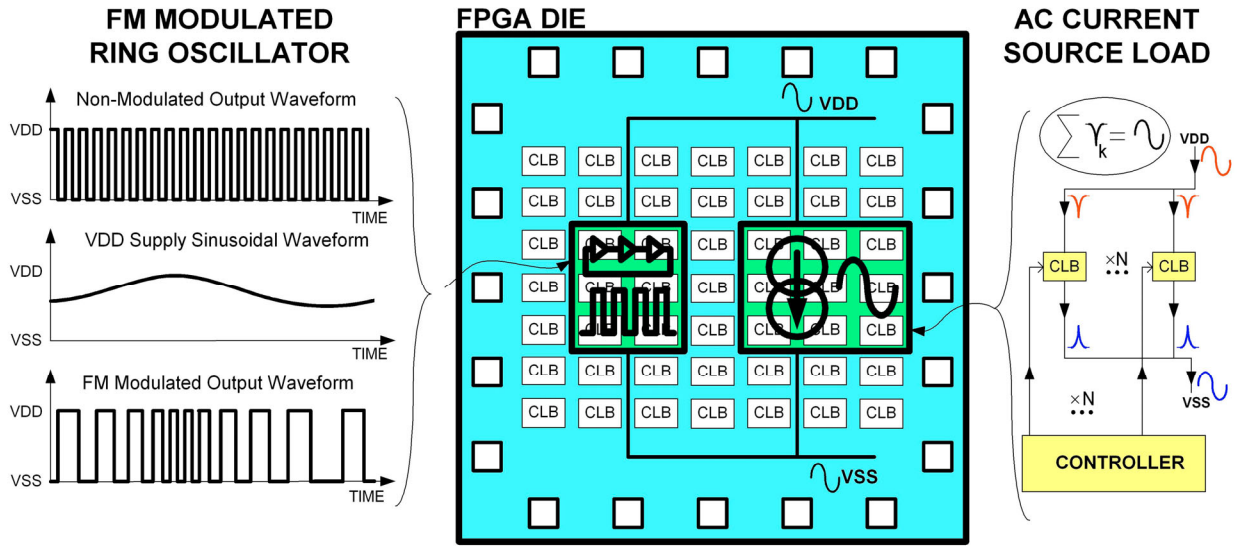

Figure 2. Block diagram of a power distribution measurement system implemented in an FPGA by configuring only commonly available logic blocks

Part of the FPGA configurable logic blocks (CLB) are configured as a current load that consumes a sinusoidal current from the on-die power supply voltage. This sinusoidal current load has programmable frequency and an activate/deactivate feature. When the current load is activated, a sinusoidal current flows through the power distribution network impedance and generates a sinusoidal variation of the on-die power supply voltage. The sinusoidal current is obtained by summing the dynamic load charging and discharging currents of multiple CMOS gates, built as part of CLB blocks, as illustrated in the right side of the figure.

Another group of configurable logic blocks of the FPGA is configured to form a ring oscillator, which is powered from the same on-die voltage supply as the sinusoidal current load.

The sinusoidal variation of the voltage supply modulates the frequency of the ring oscillator, as illustrated in the left part of the figure.

The upper trace shows the ring oscillator frequency in the absence of injected sinusoidal current. The middle trace shows sinusoidal variation of the on-die voltage supply rail due to the sinusoidal current injected into the power distribution network. The lower trace shows the frequency modulation produced by the sinusoidal variation of the voltage supply.

A frequency counter, configured also from configurable logic blocks of the FPGA, measures the steady-state average frequency of the ring oscillator signal over a period of time with and without the sinusoidal current load active. The electrical impedance of the power distribution network is then calculated using a mathematical formula involving the two measured average frequencies and functional specifications of the FPGA device. A simplified version formula could be: $Z\_PDN = [(f\_mod - f\_nom)/f\_nom] \times VDD / I\_TEST$, where Z_PDN is the power distribution impedance, f_nom is the ring oscillator frequency without injected AC current I_TEST, f_mod is the average frequency with AC injected current I_TEST, VDD is the nominal supply voltage, and I_TEST is the magnitude of the injected AC current.

By repeating this measurement at multiple frequencies of the sinusoidal current load, a frequency characteristic (frequency profile) of the power distribution impedance can be generated.

A user can remotely control this measurement process through a communication link to the FPGA. The PDN measurement block may coexist with the rest of functional cores of the FPGA, and it can be activated only when users want to measure the power distribution frequency profile. Users may store PDN impedance frequency profiles at various times along the life of the product, thus enabling comparison references with previous data when power distribution issues are suspected. Additionally, recorded PDN frequency profiles may help study any long-term reliability power distribution degradation of the system.

4. Case Study

The proposed method of PDN troubleshooting by embedded on-die impedance measurement has been implemented in a Spartan 3A FPGA on a test board. The method has been able to measure the PDN impedance frequency profile at frequencies up to 500MHz. The case study goal was to induce various failure mechanisms and to evaluate how the on-die measured frequency characteristic of the PDN impedance can be used to identify each of these failure mechanisms. The failure mechanisms induced in this test case were: open circuit tantalum capacitors, capacitance degradation in ceramic capacitors, increased interconnects series resistance, and increased loop inductance. The following sections will discuss how the proposed method detected each of these failure mechanisms.

4.1 Detecting Open Circuit Tantalum Capacitors

Tantalum capacitors tend to develop shorts through the dielectric. To avoid shorting the supply rails, manufacturers insert series fuses, thus dielectric shorts translate into open-circuit capacitors. An open-circuit tantalum capacitor failure mechanism has been induced in this test case by removing one of the two 220uF decoupling capacitors, so the resulted tantalum capacitance has been reduced to one half. The on-die PDN impedance frequency characteristic

has been measured before and after removing the capacitor. Figure 3 shows the two frequency characteristics superimposed for comparison.

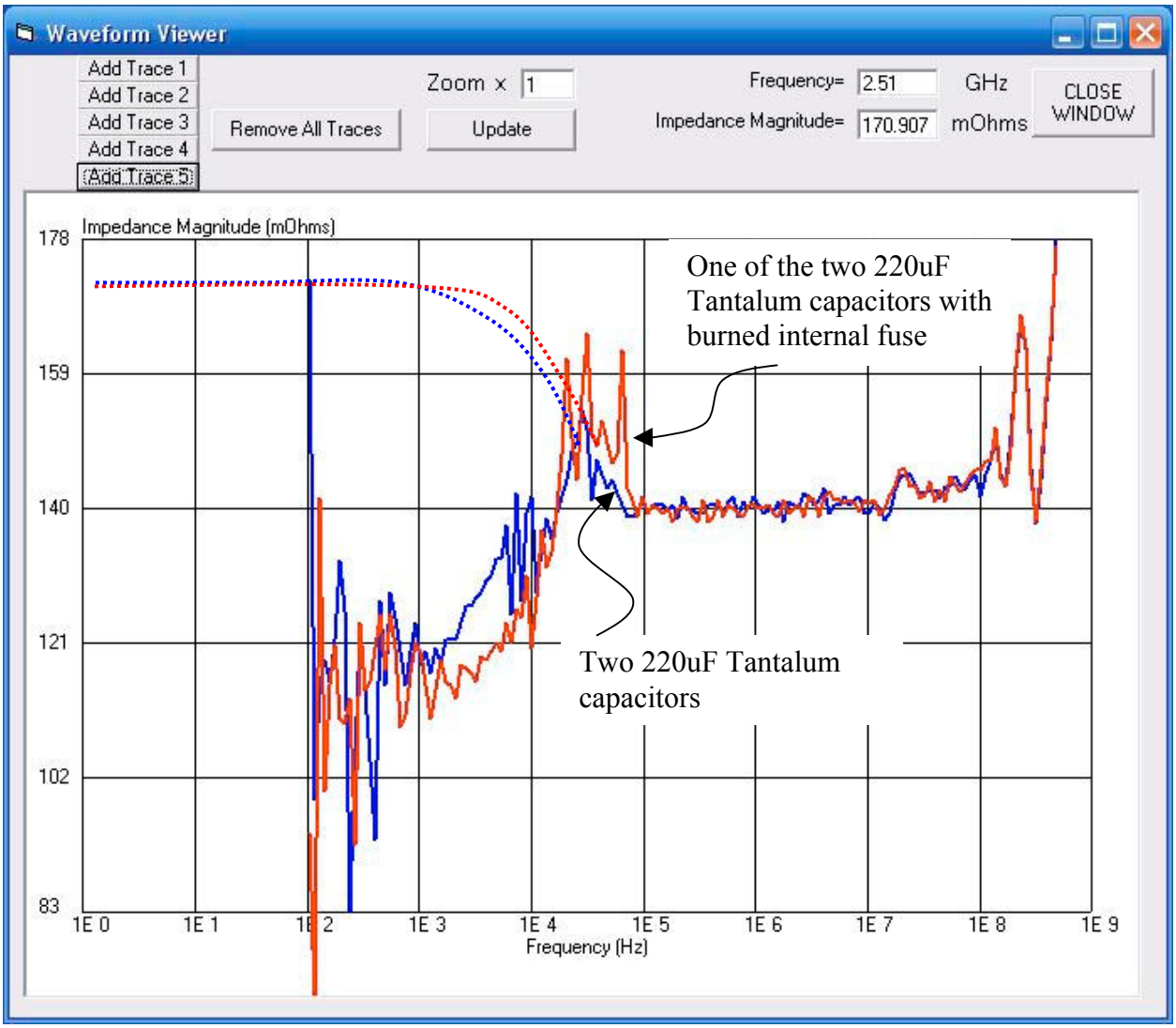

Figure 3. Frequency characteristic of PDN impedance with two functional 220uF tantalum decoupling capacitors superimposed for comparison over the frequency characteristic of PDN impedance with only one functional 220uF tantalum capacitor

The dotted line represents the expected variation of PDN impedance at lower frequencies below the accuracy frequency limit of the proposed technique. This expected PDN impedance is computed from the measured PDN impedance at zero frequency and the capacitive slope of the dominant decoupling capacitor, which in this application is the tantalum capacitor. In general the accuracy frequency limit can be extended to lower frequencies if needed with the expense of increasing the measurement time.

From the two PDN impedance traces it can be noticed that if the overall capacitance of tantalum decoupling capacitors decreases, the corresponding capacitive slope shifts horizontally towards higher frequencies. A reference PDN impedance frequency characteristic can be

recorded at product release time and it can be used later in troubleshooting work to investigate if the capacitive slope has shifted to higher frequencies. In applications with multiple tantalum decoupling capacitors, archived measurements of PDN impedance frequency characteristic can be used to study any degradation in time of decoupling capacitance caused by shorted tantalum capacitors that burn the internal fuse and become open circuits.

4.2 Detecting Capacitance Degradation in Ceramic Capacitors

Ceramic capacitors may reduce their capacitance values due to mechanical cracks in dielectric or due to dielectric aging. This failure mechanism has been induced in this test case by replacing one ceramic decoupling capacitor with 20%, 40%, 60%, and 80% lower values capacitors, so the resulted capacitance has been gradually reduced from 100% to 20%. For each capacitor value the PDN frequency characteristic has been measured and the results are shown in Figure 4.

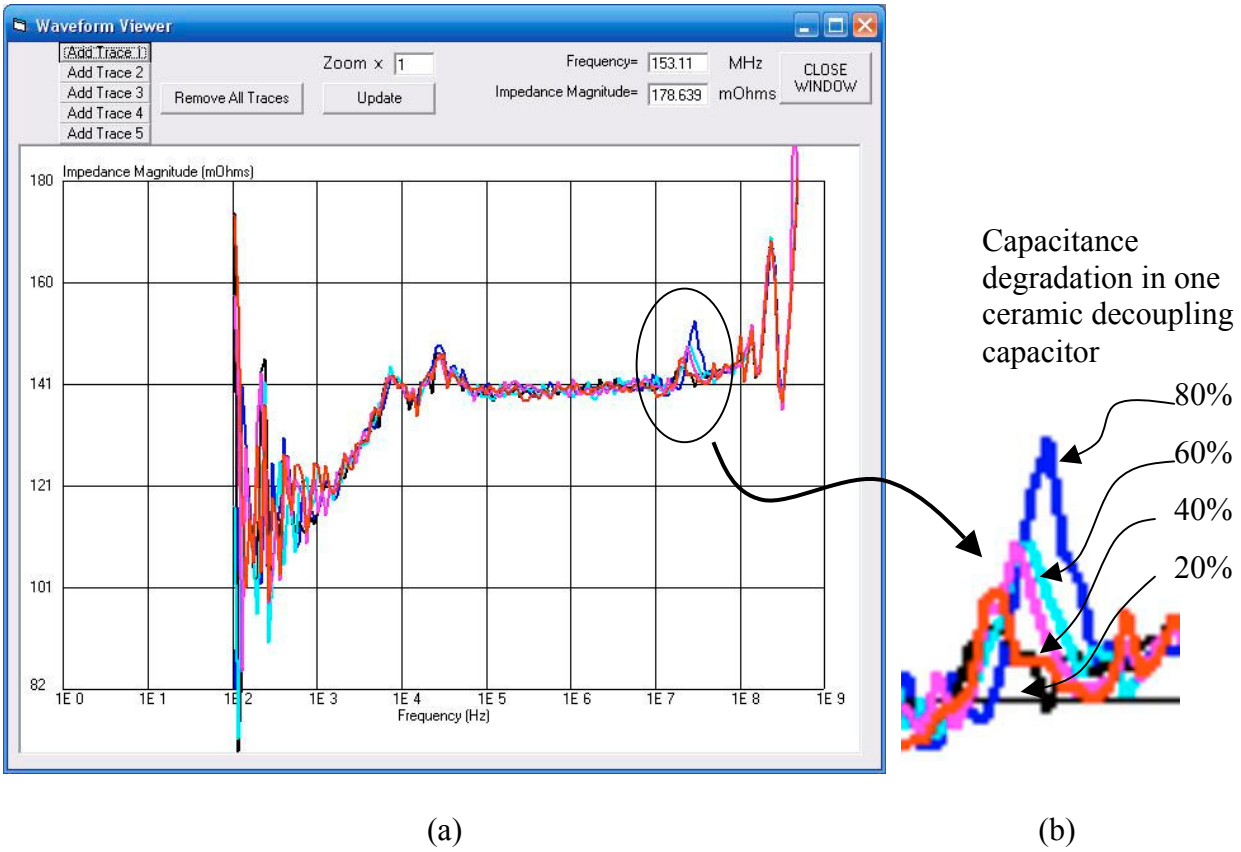

Figure 4. Ceramic capacitor degradation effects on the PDN impedance frequency characteristic (a), and magnified view of superimposed traces corresponding to 80%, 60%, 40%, and 20% capacitance degradation (b)

It can be noticed that the decrease in capacitance generates a resonant peak at about 30MHz. The magnitude of this resonance peak increases with capacitance degradation.

4.3 Detecting Increased Series Resistance of PDN Interconnects

Degradation of series resistance can result from electromigration of BGA ball interconnects, flip-chip solder bumps, and die bond wires, or increased resistance of vias and interconnects on PCB. This failure mechanism has been induced in this test case by partially cutting the electric current path of a group of power supply vias to the FPGA BGA package. Figure 5 shows the effects of increasing resistance to the PDN impedance frequency characteristic.

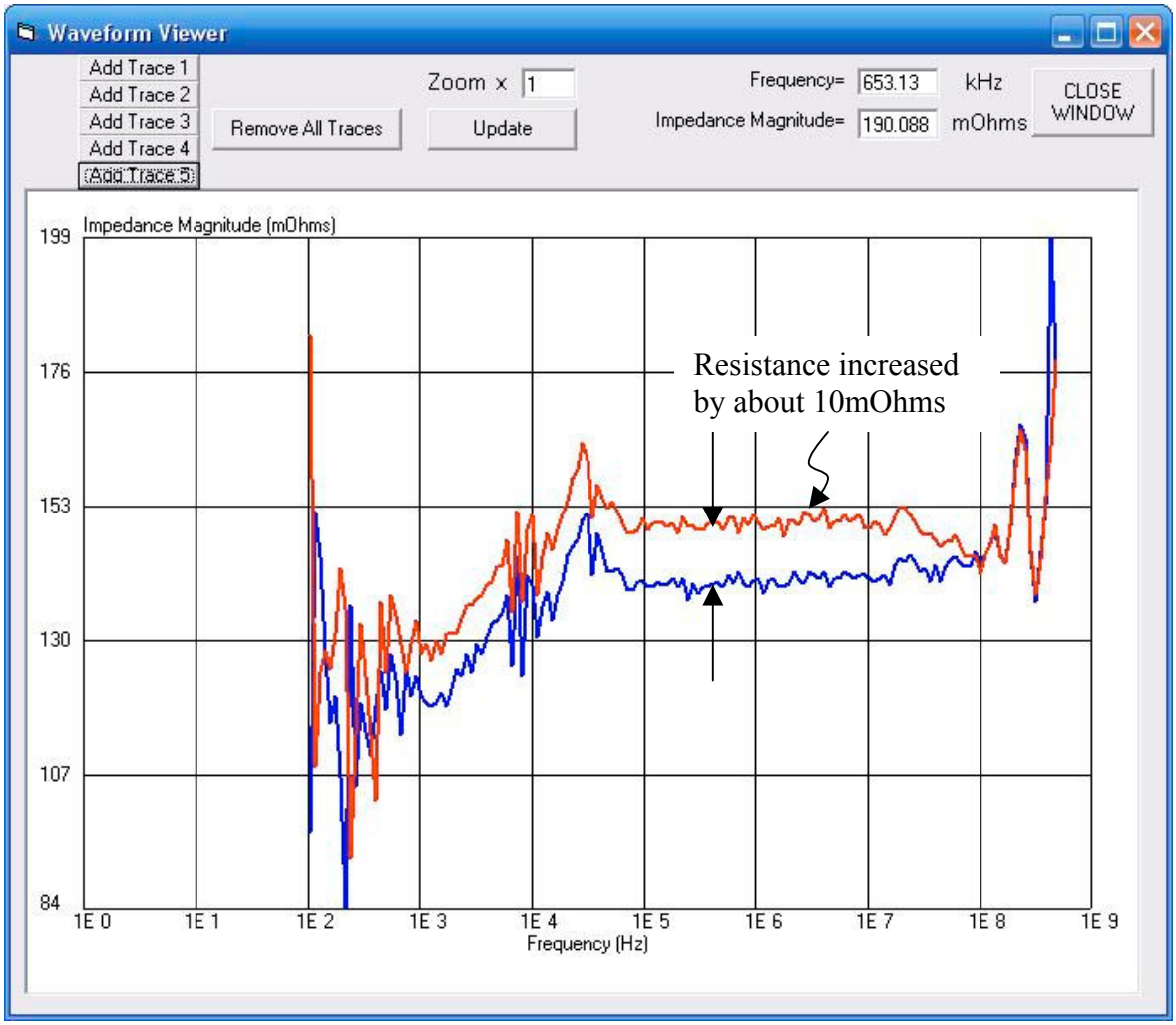

Figure 5. Effects of increasing interconnect resistance to the PDN impedance frequency characteristic.

The blue trace (lower trace) has been shifted up about 10mOhms as the effect of increasing the PDN series resistance. It can be noticed that this vertical shift disappears at around 100MHz. This result is expected since as frequency increases the majority of AC current closes through the decoupling capacitors on the package and die, and therefore, the dominant current does not flow through the increased resistance section of the PDN on PCB.

The frequency where the resistive shift disappears can provide information about where in the overall power distribution network of the system the series resistance has increased, this

way making possible to identify failing connectors, sockets, or electromigration degradation on PCB, in the package, or in the die.

4.4 Detecting Increased Loop Inductance

Degradation of PDN in the form of open circuit paths (like part of the vias on a power supply rail, part of the pins of a connector, or part of the decoupling capacitors on a supply rail) typically does not result in total PDN failure because there exist alternate paths for current to flow. However, these open circuit paths redistribute the transient or AC current flow throughout the power distribution network circuitry. As a direct consequence, the overall loop inductance of the power distribution network increases. This increase is typically selective, being more significant at some frequencies and negligible at other frequencies.

This failure mechanism has been induced in this test case by blocking the AC current flow through one ceramic capacitor, thus forcing the current to find alternate paths to flow. Figure 6 show the effects of current redistribution to the PDN impedance frequency characteristic.

Figure 6. Effects of current redistribution to the PDN impedance frequency characteristic

The blue trace (lower trace) represents the original PDN impedance and the red trace (upper trace) represents the PDN impedance with redistributed current flow. It can be noticed the dominant resonance peak that appears at around 8MHz, but it can also be noticed the increased impedance over the frequency range between about 400kHz and 4MHz. This increased impedance results from part of the AC current flowing through a different path that has a larger loop inductance than the original path.

Other failure mechanisms may be investigated in similar ways, and troubleshooting of PDN impedance may be done by comparing the measured PDN impedance frequency characteristic with previously archived measurements or just with expected PDN frequency characteristics.

5. Conclusion

This paper has presented a method for troubleshooting power distribution network (PDN) issues in new or existing electronic systems by embedded measurement of power distribution impedance in programmable logic devices (PLD) such as FPGAs and CPLDs. The proposed troubleshooting method has all measurements done internally inside the PLD with the only need of a communication link with the programmable logic device (which typically is already in place in most electronic systems). Therefore, this method can be easily implemented in existing production test floors, in product support/repair environments, or to remotely troubleshoot systems installed in the field in hardly accessible areas. Programmable logic devices can have implemented the PDN measurement system all the time, or they can be only temporarily configured to measure the power distribution impedance after which they can be reconfigured back to their previous functionality. A test case has been used to evaluate this method on intentionally induced failure mechanisms: open circuit tantalum capacitors, capacitance degradation in ceramic capacitors, increased series resistance of interconnects, and increased loop inductance. Measurement results and further analysis has demonstrated that the proposed method can successfully identify each of these failure mechanisms.

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