# Contents

1 FUNDAMENTAL CONCEPTS 1

1.1 What is Noise Coupling 1

1.2 Resistance 3
  1.2.1 Resistivity and Resistance 3
  1.2.2 Wire Resistance 4
  1.2.3 Sheet Resistance 5
  1.2.4 Skin Effect 6
  1.2.5 Resistance of Semiconductors 7

1.3 Resistive Coupling 9
  1.3.1 Resistive Coupling in Lightly Doped Substrates 10
  1.3.2 Resistive Coupling in Heavily Doped Substrates 11
  1.3.3 Resistive Coupling Through Voltage Drops 12

1.4 Inductance 13
  1.4.1 Electric Current Flowing Through a Wire 13
  1.4.2 Conductive Wire Encircled by Magnetic Field 14
  1.4.3 Time Varying Current Flowing Through a Wire 15
  1.4.4 Self-Inductance of a Straight Wire Segment 16

1.5 Inductive Coupling 19
### Contents

#### 1 Inductance

- 1.5.1 Mutual Inductance ........................................... 19
- 1.5.2 Total Inductance ........................................... 21
- 1.5.3 Loop Inductance ........................................... 22
- 1.5.4 Loop Mutual Inductance ................................... 24

#### 1.6 Capacitance

- 1.6.1 Parallel Plate Capacitor .................................... 26
- 1.6.2 Semiconductor Junction Capacitance ...................... 27

#### 1.7 Capacitive Coupling

- 1.7.1 Wire to Wire Capacitive Coupling ......................... 31
- 1.7.2 Decoupling Capacitors ..................................... 32

#### 2 INTEGRATED CIRCUITS FABRICATION

- 2.1 Introduction ..................................................... 37

#### 2.2 Integrated Circuits Fabrication Technology

- 2.2.1 Wafer Manufacturing ....................................... 38
- 2.2.2 Device Manufacturing ...................................... 39
- 2.2.3 Bipolar Process ............................................ 43
- 2.2.4 CMOS Process ............................................. 50
- 2.2.5 BiCMOS Process ........................................... 59
- 2.2.6 Silicon on Insulator (SOI) Process ......................... 60

#### 2.3 Packaging Technology

- 2.3.1 Wire Bonding Package ..................................... 62
- 2.3.2 Tape Automated Bonding Package ......................... 62
- 2.3.3 Flip-Chip Package ......................................... 63

#### 2.4 Printed Circuit Boards Technology ......................... 65

#### 2.5 Power Distribution

- 2.5.1 Power Distribution Model .................................. 67
- 2.5.2 Decoupling Capacitors .................................... 70
- 2.5.3 Example of a Power Distribution Model .................. 73

#### 3 MECHANISMS OF NOISE GENERATION

- 3.1 Introduction ..................................................... 75

#### 3.2 Substrate Noise Generation

- 3.2.1 NPN Transistor in Common-Emitter Configuration ...... 77
- 3.2.2 NPN Transistor in Cascode Configuration ................ 79
- 3.2.3 NPN Transistor inEmitter-Follower Configuration ....... 80
7 NOISE COUPLING SUPPRESSION 199

7.1 Introduction 199

7.2 Suppression of Noise Generation 200
  7.2.1 Differential CMOS Logic 200
  7.2.2 Single Ended Current Steering CMOS 201
  7.2.3 Current Balanced CMOS 203
  7.2.4 Supply Current Shaping 204
  7.2.5 Power Distribution Impedance 205

7.3 Suppression of Noise Propagation 212
  7.3.1 Using Lightly Doped Substrates Instead of Heavily Doped 212
  7.3.2 Buried Substrate Shields: Faraday Shield 213
  7.3.3 Buried Substrate Shields: Dielectric Shield (SOI process) 215
  7.3.4 Buried Substrate Shields: Junction Shield 217
  7.3.5 Shunting Guard Rings 218
  7.3.6 High Resistance Guard Rings 220
  7.3.7 Active Guard Rings 221

7.4 Suppression of Noise Reception 223
  7.4.1 Differential Versus Single Ended Circuits 223
  7.4.2 Shunting Through Substrate Contacts 226
  7.4.3 Circuit Level Compensation 227

7.5 Design Example 1: Circuit Level Compensation for Substrate Noise Coupling in Common-Source NMOS Amplifier 228
  7.5.1 Architecture and Functionality 228
  7.5.2 Experimental Results 231

7.6 Design Example 2: Circuit Level Compensation for Substrate Noise Coupling in NMOS Active Loads 233
  7.6.1 Architecture and Functionality 233
  7.6.2 Experimental Results 235

8 NOISE COUPLING SIMULATION 239

8.1 Introduction 239

8.2 Using Software Simulation Tools 240
  8.2.1 Overview of Noise Coupling Simulation 240
  8.2.2 Post-Layout Extraction and Simulation 241
  8.2.3 Pre-Layout Extraction and Simulation 242
  8.2.4 Early Estimation in the Architectural Stage of the Design 243
8.3 Early Prediction of Noise Coupling 244
8.3.1 Modeling Requirements 244
8.3.2 Modeling Assumptions 245
8.3.3 Methodology 246
8.3.4 Estimation of the Digital Switching Noise 247
8.3.5 Two-Dimensional Analog Mesh 251
8.3.6 Alternate One-Dimensional Analog Mesh 255
8.3.7 Digital Circuits, Package, and PCB Power Distribution 257

8.4 Example of Early Prediction of Noise Coupling 259
8.4.1 Model Construction 259
8.4.2 Simulation Results and Correlation with Measurements 260