ChipQuake™ Power Integrity Explorer User Guide

Learning Edition
Version 1.1

NoiseCoupling.com

Contents

ChipQuake™ Power Integrity Explorer User Guide

Introduction

This user guide is intended to provide the user with the basic knowledge needed to setup and run **ChipQuake™ Power Integrity Explorer** simulations.

ChipQuake™ Power Integrity Explorer Overview

ChipQuake™ provides fast frequency domain simulations of power integrity and noise coupling in mixed signal integrated circuits, including the effects of package and printed circuit boards (PCBs). **ChipQuake™** allows design engineers and system architects to visualize power integrity and noise coupling tradeoffs in a chip/package/PCB co-design.

ChipQuake™ can be used to:

- Analyze the power integrity on the chip, package, and printed circuit board (PCB)
- Analyze the noise coupling effects on the analog regions of mixed-signal integrated circuits.
- Examine various floor-plan options, pin assignments, power grid sizes, and guard ring isolations.
- Analyze the effects of various packaging options on noise coupling.
- Explore decoupling capacitor types, values, and placement locations on the chip, package, and PCB.

INPUTS
ChipQuake™ uses the information available in the design specifications, technology manual, package datasheet or specifications, and statistical data from typical design practices or previous designs.

OUTPUTS
ChipQuake™ generates two- and three-dimensional color coded maps of the substrate and power supply noise. Mouse move probing displays the noise voltage function of X-Y coordinates. ChipQuake™ generates also frequency sweep characteristics of power supply rails on the chip, package, and PCB, and noise coupling at any X-Y coordinate in the analog region of mixed signal integrated circuits.

SIMULATION TIME
ChipQuake™ is a fast simulator. Most simulations take less than one minute.

ACCURACY
The estimation accuracy is lower compared to that provided by post- and pre-layout extraction and simulation tools but good enough to analyze the major physical mechanisms that contribute to power integrity and noise coupling degradation in integrated circuits.

System Requirements

This section presents a set of minimum recommended system requirements for installing and running the ChipQuake™ simulation software.

Windows XP SP2

RAM 500Mb

Hard Disk available memory 10Mb

CPU 1GHz

Display 1024 by 768

Available CDROM drive

Installation Instructions

Backup all the important data and create a system restore point in case you will want to uninstall the ChipQuake™ software in the future.

It is recommended to exit all the running applications before starting the ChipQuake™ installation.

Insert the ChipQuake™ installation disk in a CDROM drive. The ChipQuake™ installation program will run automatically. If not, open the ChipQuake™ folder and run the Setup.exe application.

Follow the on-screen instructions to complete the installation.

If in the future you decide to uninstall the ChipQuake™ software, you may use the "Add/Remove programs" utility available in the "Control Panel" of the Windows operating system. It is recommended to uninstall the demo version before installing to full version.

Running ChipQuake

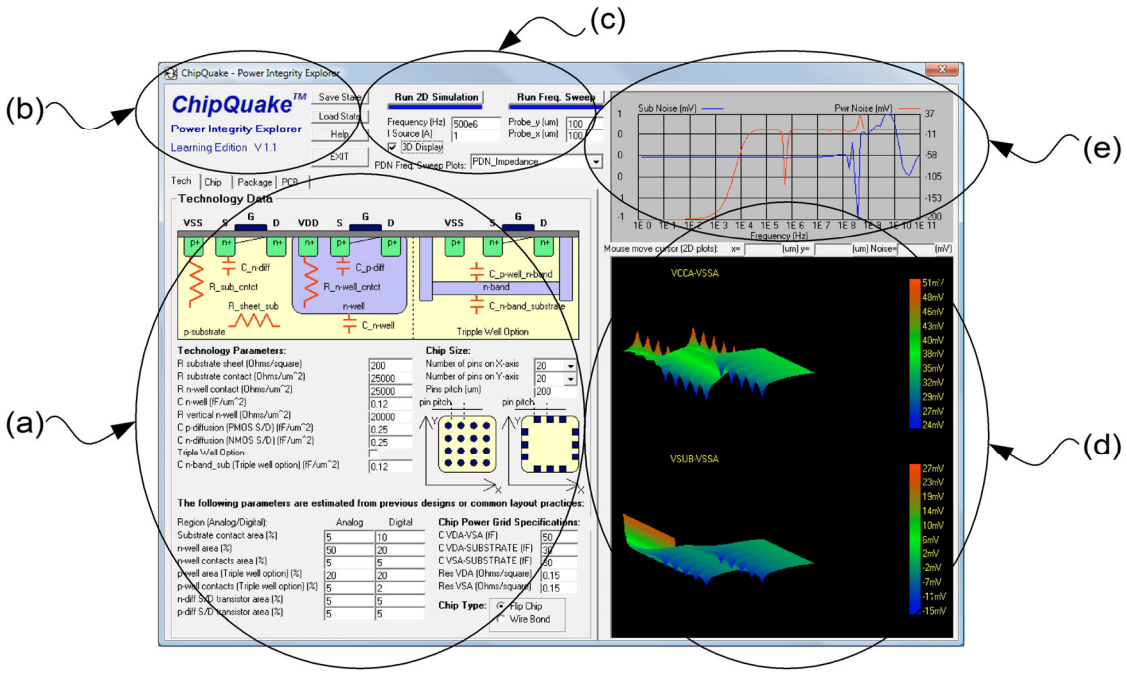
ChipQuake™ starts with a simulation run using default design parameters, which typically takes less than one minute. This simulation has two parts, a two-dimensional mesh simulation, and a frequency sweep. Two blue color status bars monitor both simulations. Details about setting up and running these simulations will be presented later in this user guide.

Important: If the ChipQuake™ window or other windows are moved or resized during the simulation, the results are not displayed. When this happens, restart the simulation by pressing the "2D Mesh Simulation" and then the "Freq. Sweep" control buttons.

After the "start-up" simulations are completed, the program is ready to be used.

ChipQuake Graphical User Interface

ChipQuake™ has a single window panel, which is used to setup, run, and view the simulation results. The following figure shows a picture of the ChipQuake™ graphical user interface panel.



Design Input Section

The design input section is marked by label (a) in the figure above. This section contains four frames selectable through the TAB-STRIP control buttons at the top. The four sections are: Technology Data (labeled "Tech" on the Tab-Strip selection buttons), Chip Design Parameters (labeled "Chip" on the Tab-Strip selection buttons) , Package Design Parameters (labeled "Package" on the Tab-Strip selection buttons), and PCB Design Parameters (labeled "PCB" on the Tab-Strip selection buttons).

Load and Save Section

The load and save section are marked by label (b). This section has a control button that allows the user to save the design input parameters into a file, and a second control button that allows the user to load the design input parameters previously stored in a file. This section contains also the control button for exiting the ChipQuake™ program.

Simulation Setup and Run Section

The simulation setup and run section is marked by label (c). This section contains the simulation parameters and the buttons for starting simulations. There are two types of simulations: AC simulation of the entire analog region two-dimensional mesh model at a single frequency, and AC frequency sweep at a single location point in the analog region.

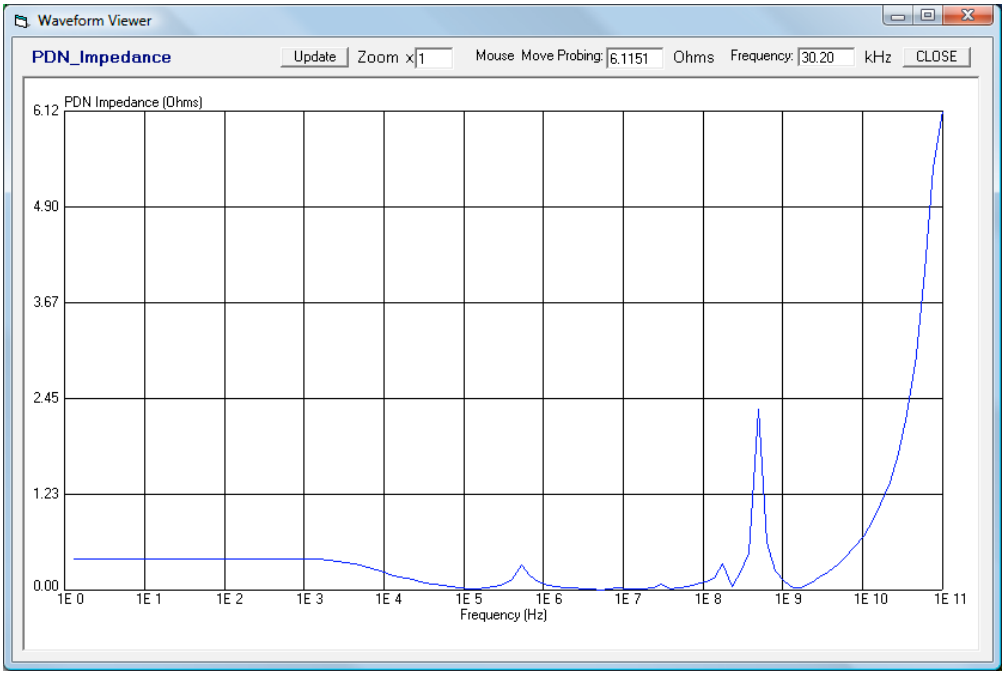
Results Section for Two-dimensional Mesh Simulations

The results section for distributed mesh simulation results is marked by label (d). This section displays two or three dimensional maps of the power supply and substrate noise at each location in the simulated region of the chip.

Results Section for Frequency Sweep Simulations

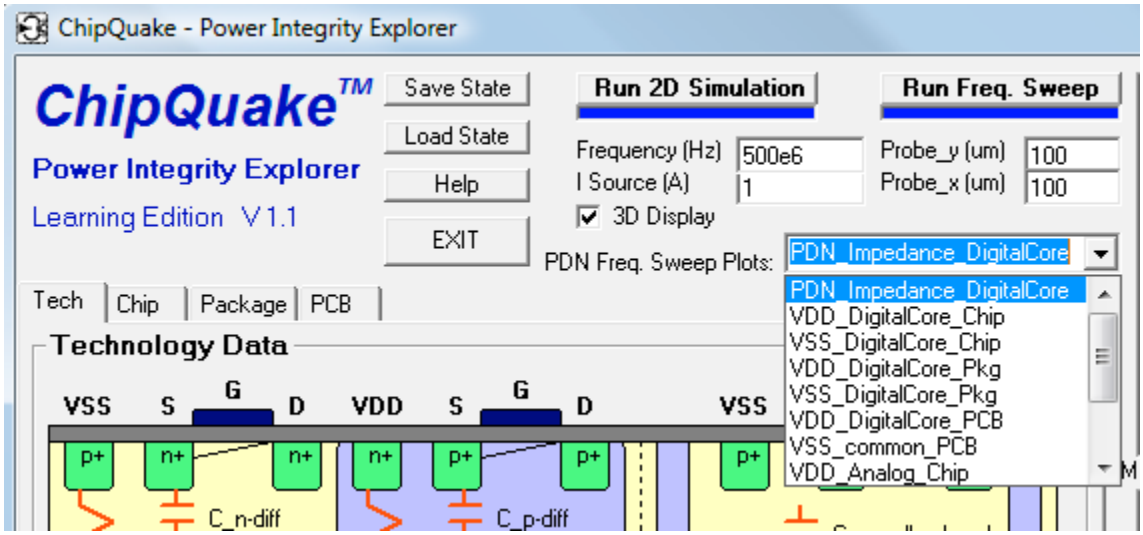
The results section for frequency sweep simulations is marked by label (e). This section displays the power supply and substrate noise frequency spectrum at a selectable single location in the simulated region of the chip.

An second window shows the frequency sweep results for the power distribution network as seen from the on-chip circuits, as shown in the following figure:



On the top region of this waveform viewer window there is an “Update” button, a Zoom control text box, and a mouse-move cursor that displays the frequency and amplitude value at the mouse cursor location.

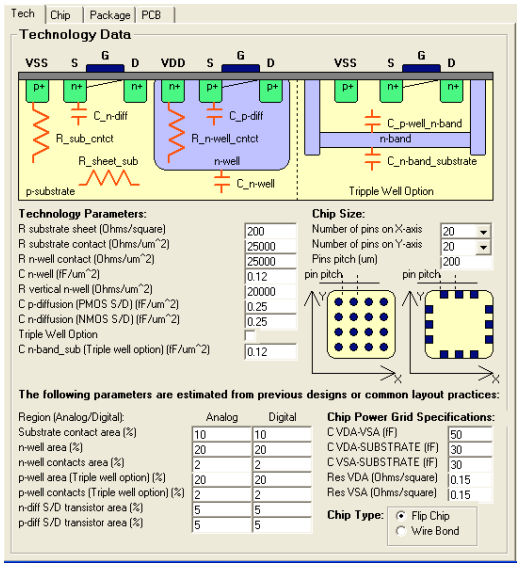
The waveform viewer window can display also the frequency sweep results for the on-chip, on-package, and on-PCB analog and digital power rails. The display selection is done through a multiple-choice select box on the main ChipQuake window, as shown in the figure below:



Design Data Entry

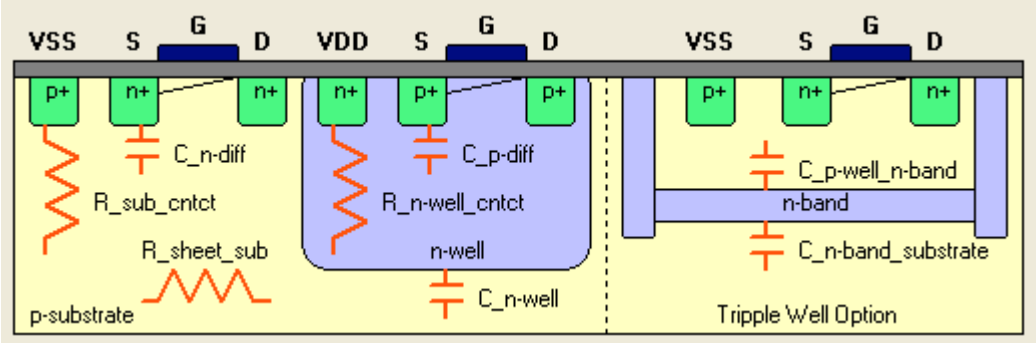
Technology Data Frame

The technology data frame can be invoked by clicking on the corresponding button in the TAB-STRIP control, located on the upper left corner of the data input section.



The technology data frame consists of a symbolic drawing of a typical CMOS process, and data entry sections for technology parameters, chip type and size, and statistical parameters estimated from previous designs or common layout practices.

The symbolic drawing, shown in detail below defines graphically some of the technology parameters specific to CMOS processes.



These parameters are typically found under various names in the design manual of each fabrication process. The drawing has been inserted in this frame to simplify the identification of each technology parameter in the design manual.

The values of these parameters are entered in the "Technology Parameters" section, shown below.

Technology Parameters:

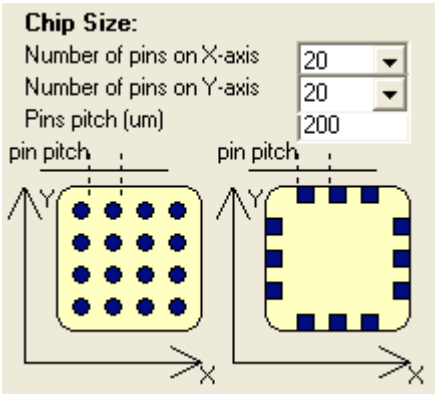
R substrate sheet (Ohms/square)	200
R substrate contact (Ohms/um^2)	25000
R n-well contact (Ohms/um^2)	25000
C n-well (fF/um^2)	0.12
R vertical n-well (Ohms/um^2)	20000
C p-diffusion (PMOS S/D) (fF/um^2)	0.25
C n-diffusion (NMOS S/D) (fF/um^2)	0.25
Triple Well Option	☐
C n-band_sub (Triple well option) (fF/um^2)	0.12

If the chip is fabricated on a bulk substrate, the "Triple Well Option" button remains unselected. If the chip is fabricated on a substrate with isolated p-wells and n-wells, the "Triple Well Option" button needs to be selected. In this case the value of the n-band capacitance needs to be entered.

Important: The numerical values need to be entered in the same format as shown by the default parameters. If an unsupported numerical format is entered or if a spelling mistake is made, the ChipQuake™ program runs into an error state and automatically terminates without any warning. If this happens, all the unsaved parameter values are lost. Next run of ChipQuake™ starts with the default parameter values.

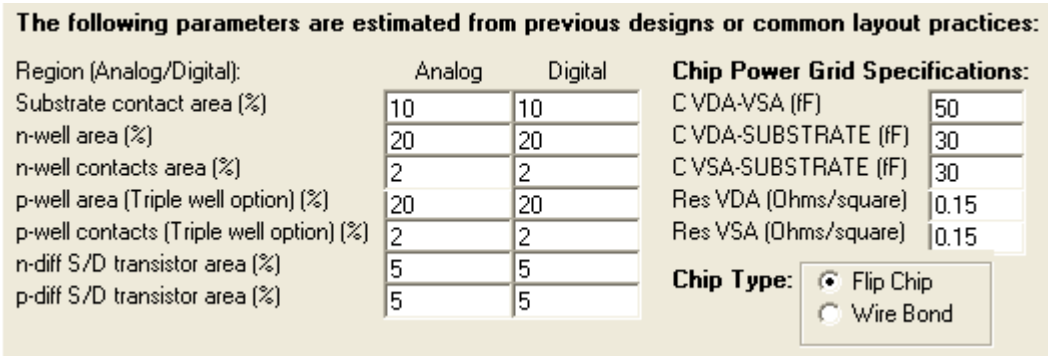
Chip Size

The width and height of the chip need to be entered as the number of pins and the spacing between the pins. The spacing between pins is also known as pin pitch. This is illustrated graphically by the two drawings representing a flip-chip and a wire-bond chip.



Statistical Parameters

The figure below shows the frame region used for entering statistical design parameters estimated from common design practices or previous projects. These statistical parameters are needed to overcome the unavailable layout information in the early stages of the design flow.

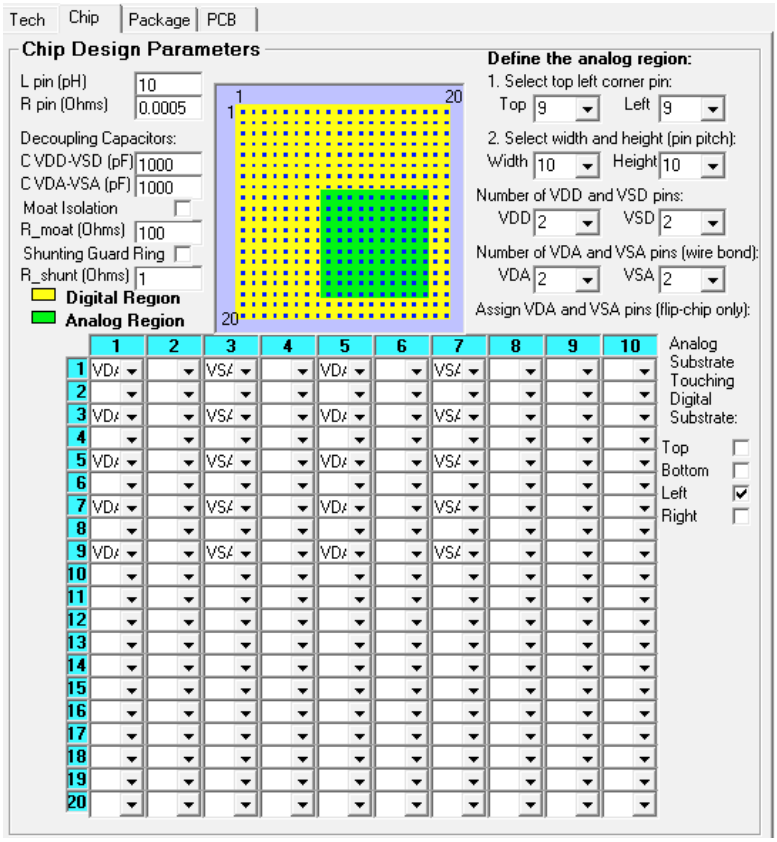


The left side shows the entries for the estimated area percentages of substrate contacts, n-wells, n-well contacts, p-wells, p-well contacts, source and drain diffusions of NMOS transistors, and source and drain diffusions of PMOS transistors. Each statistical parameter has two entries: one for the analog region and one for the digital region. The right side shows the entries for the estimated power grid parasitic resistance and capacitance. These values can be calculated or extracted from the chip power grid or from a preliminary version, if the final version is not available in the early stages of the design.

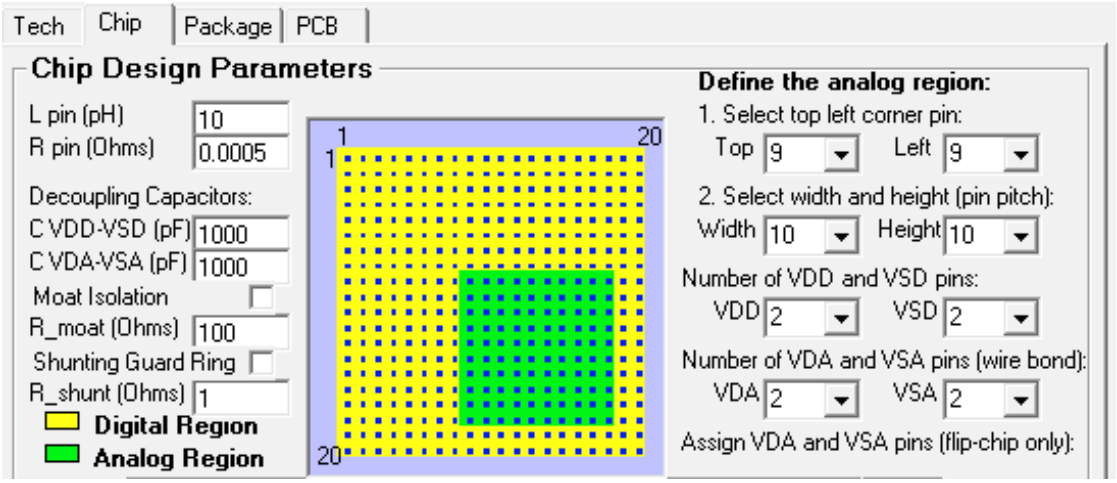
Important: The numerical values need to be entered in the same format as shown by the default parameters. If an unsupported numerical format is entered or if a spelling mistake is made, the ChipQuake™ program runs into an error state and automatically terminates without any warning. If this happens, all the unsaved parameter values are lost. Next run of ChipQuake™ starts with the default parameter values.

Chip Data Input Frame

The chip data input frame can be invoked by clicking on the corresponding button in the TAB-STRIP control, located on the upper left corner of the data input section.



The top left region contains entries for the inductance and resistance of the pins. This information is typically available in the fabrication technology design guide. The following entries are intended for the on-chip decoupling capacitance in the digital and in the analog regions. Next, there are selection buttons and parameter value entries for high resistive moat or shunting guard ring isolation techniques, if any of them are implemented on the chip.



The top right region defines the physical placement and the size of the analog region in the overall floorplan of the chip. The physical placement is entered by the coordinates of the top-left corner measured in pin pitch units. The example shown in the figure above marks the top-left corner as the Top=6 and Left=9, which means that the analog region top left corner starts at pin 6 on the vertical axis and pin 9 on

the horizontal axis. The following "Width" and "Height" entries define the size of the analog region, also in pin pitch units. The figure in the center shows graphically the location and size of the analog region.

The following entries define the number of power supplies pins in the digital region, VDD and VSD, and in the analog region, VDA and VSA.

For wire-bond chips, the locations of the power supply pins are not specified, instead they are assumed uniformly distributed around the perimeter of the chip.

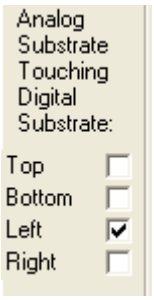
For flip-chip designs, the locations of the power supply pins are entered using the array diagram shown in the following figure.

The pins coordinates are referenced to the analog region, and not to the overall chip. In the example above, pin (1,1) corresponds to pin (9,6) of the overall chip, where 9 is measured on the horizontal axis and 6 on the vertical axis.

To assign power or ground pins to a specific location, right-click with the mouse on the arrow select option corresponding to the chosen coordinate and select: "VDA" for positive supply, "VSA" for negative supply, or blank space for any other type of signal. Due to font size limitations, the displayed pin type shows "VD" for the "VDA", and "VS" for the "VSA".

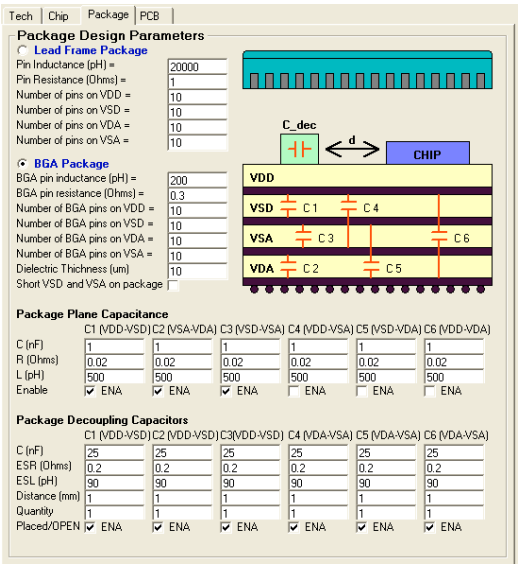
Important: The text box entries for pin types accept typed characters besides the pre-selected "VDA", "VSA", and blank space. Do not type any characters in these text boxes. Choose only from the pre-selected options. Typing any characters may generate errors in the program execution and automatically terminate ChipQuake™ without any warning. If this happens, all the unsaved parameter values are lost. Next run of ChipQuake™ starts with the default parameter values.

Depending on the size and physical location, the analog region may interface with the rest of the chip on one side, two sides, three sides, or all four sides. This information is entered using the checkbox selections shown in the following figure.

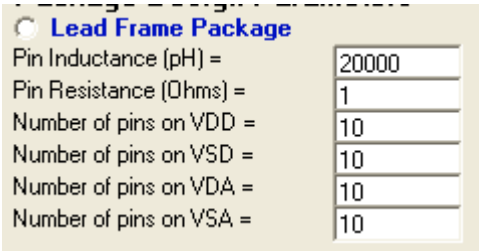


Package Data Input Frame

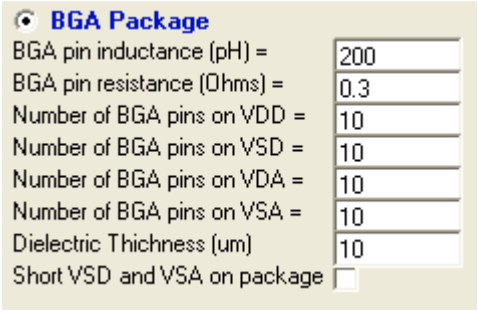
The package data input frame can be invoked by clicking on the corresponding button in the TAB-STRIP control, located on the upper left corner of the data input section.



If the chip is placed on a lead-frame type package, enter the pin inductance, pin resistance, and number of pins on each supply as shown in the following figure.

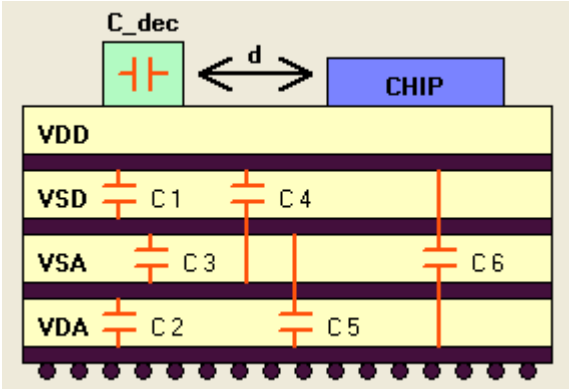


If the chip is placed on a BGA type package, enter the pin inductance, pin resistance, number of pins on each supply, and dielectric thickness as shown in the following figure. If a common ground plane is used for both analog and digital grounds of the chip, check the "Short VSD and VSA on package" box.

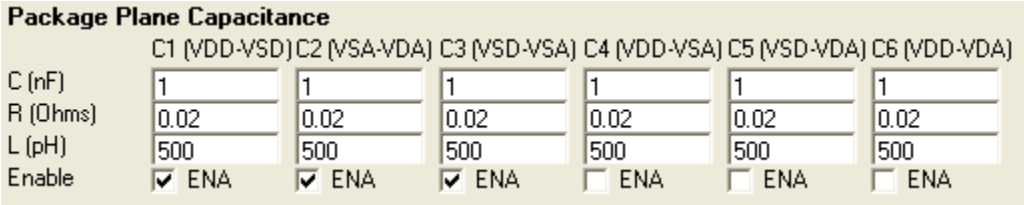


Important: The numerical values need to be entered in the same format as shown by the default parameters. If an unsupported numerical format is entered or if a spelling mistake is made, the ChipQuake™ program runs into an error state and automatically terminates without any warning. If this happens, all the unsaved parameter values are lost. Next run of ChipQuake™ starts with the default parameter values.

For BGA packages the parasitic plane capacitance, resistance, and inductance need to be entered. The following figure illustrates graphically the definition of the plane capacitances, C1 – C6.

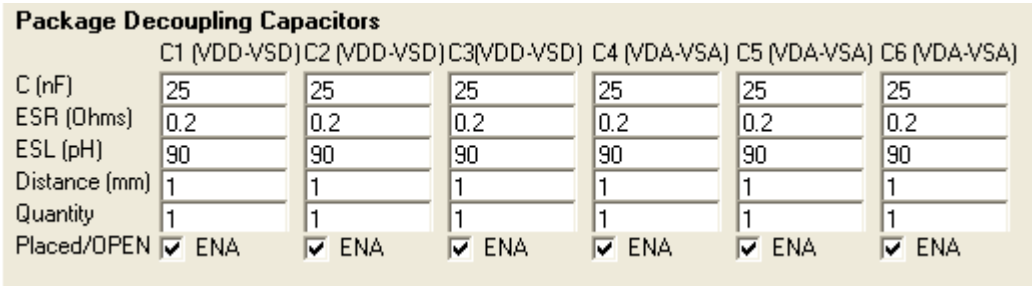


Depending on the physical stackup layer definition, only some of these capacitances exist. Use the checkbox labeled "Enable" as shown in the following figure to activate the corresponding capacitances. Leave unchecked the capacitances that do not exist in the stackup. Then enter the capacitance value, parasitic resistance, and parasitic inductance.



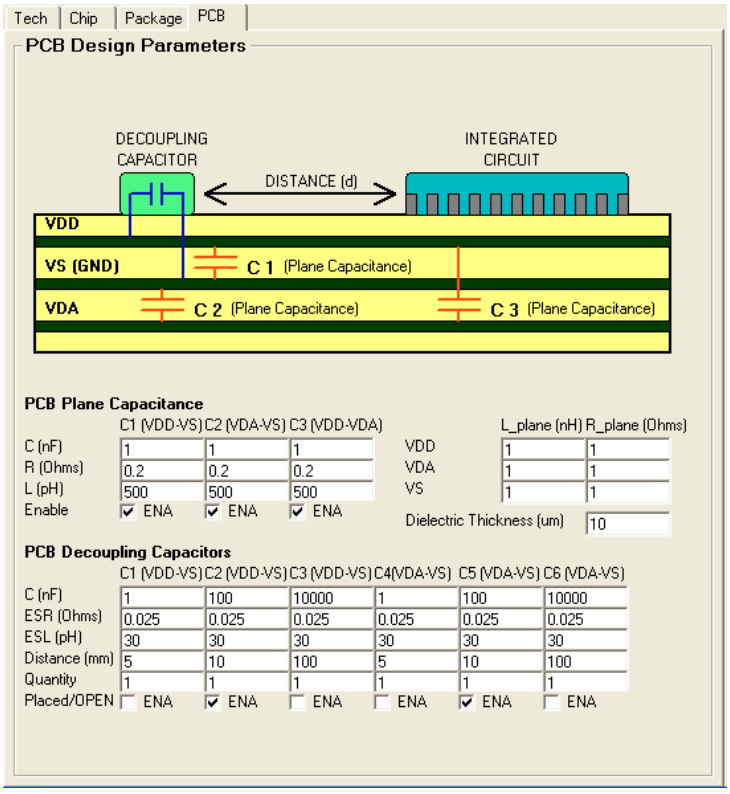
Some BGA packages implement decoupling capacitors. Enter the capacitor parameters as shown in the following figure. The first three columns represent decoupling capacitors on the digital power supply, and

the other three columns represent decoupling capacitors on the analog power supply. The "Distance" represents the physical separation between the capacitor and the chip, as defined in the drawing of the chip.

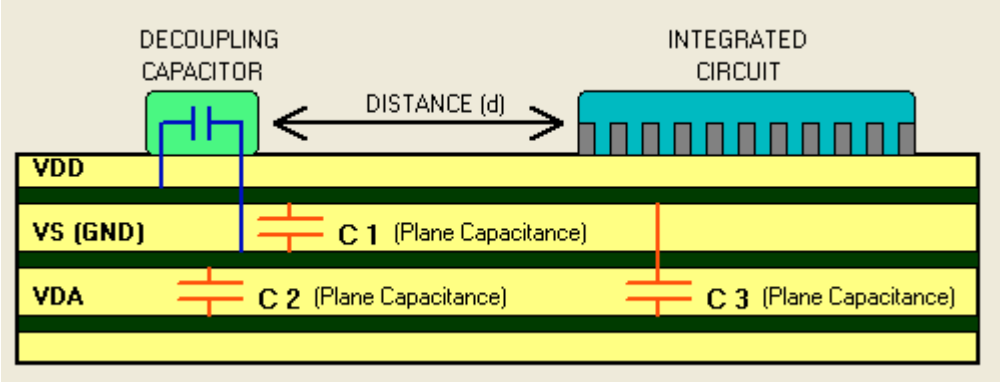


PCB Input Frame

The PCB data input frame can be invoked by clicking on the corresponding button in the TAB-STRIP control, located on the upper left corner of the data input section.



The top drawing illustrates graphically some of the definitions and notations used in the data entry fields..



Depending on the power planes assignment in the physical stackup of the PCB, not all the plane capacitances exist. Use the checkbox labeled "Enable" as shown in the following figure to activate the corresponding capacitances. Leave unchecked the capacitances that do not exist in the stackup. Then enter the capacitance values, parasitic resistances, and parasitic inductances.

PCB Plane Capacitance

	C1 (VDD-VS)	C2 (VDA-VS)	C3 (VDD-VDA)
C (nF)	1	1	1
R (Ohms)	0.2	0.2	0.2
L (pH)	500	500	500
Enable	☑ ENA	☑ ENA	☑ ENA

	L_plane (nH)	R_plane (Ohms)
VDD	1	1
VDA	1	1
VS	1	1

Dielectric Thickness (um): 10

The data entry fields in the right side represent the inductance and resistance of the PCB power planes and the dielectric thickness.

Various decoupling capacitors are placed on the PCB in the immediate vicinity of the integrated circuit. Enter the capacitor parameters as shown in the following figure. The first three columns represent decoupling capacitors on the digital power supply, and the other three columns represent decoupling capacitors on the analog power supply. The "Distance" represents the physical separation between the capacitor and the integrated circuit, as defined in the drawing of the chip.

PCB Decoupling Capacitors

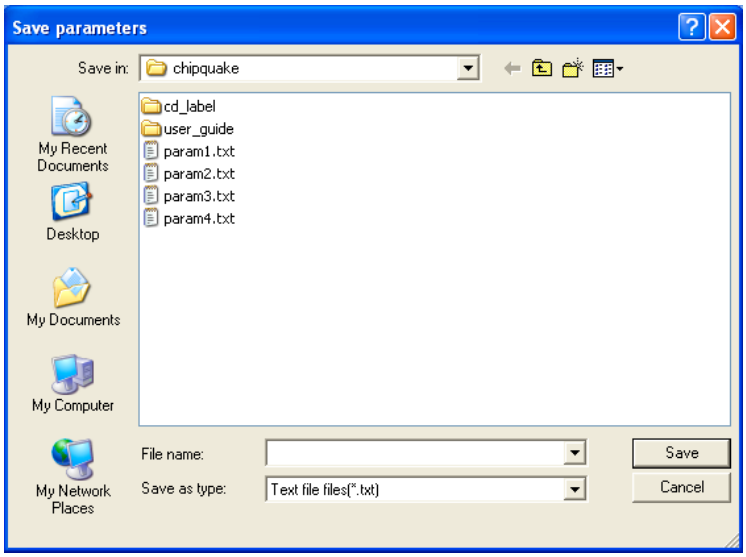
	C1 (VDD-VS)	C2 (VDD-VS)	C3 (VDD-VS)	C4(VDA-VS)	C5 (VDA-VS)	C6 (VDA-VS)
C (nF)	1	100	10000	1	100	10000
ESR (Ohms)	0.025	0.025	0.025	0.025	0.025	0.025
ESL (pH)	30	30	30	30	30	30
Distance (mm)	5	10	100	5	10	100
Quantity	1	1	1	1	1	1
Placed/OPEN	☐ ENA	☑ ENA	☐ ENA	☐ ENA	☑ ENA	☐ ENA

Important: The numerical values need to be entered in the same format as shown by the default parameters. If an unsupported numerical format is entered or if a spelling mistake is made, the ChipQuake™ program runs into an error state and automatically terminates without any warning. If this happens, all the unsaved parameter values are lost. Next run of ChipQuake™ starts with the default parameter values.

Save and Load Functions

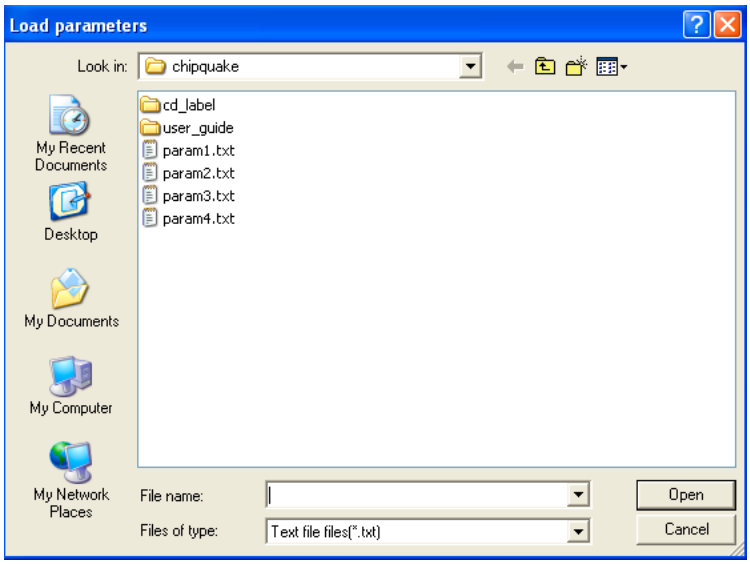
Saving the Design Parameters

The design parameters can be saved at any time by clicking on the "Save State" button located in the top left region of the user interface panel. When the save parameters dialog box opens, choose a working directory and type a name for the parameter file. The file type must have text format, as shown by "param1.txt" – "param4.txt" in the example below.



Loading Previously Saved Design Parameters

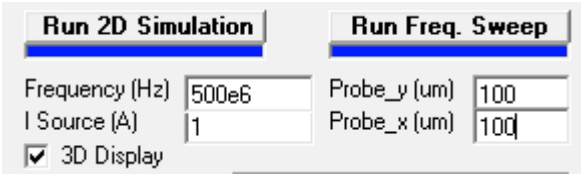
Previously saved parameter files can be loaded at any time by clicking the "Load State" button located in the top left region of the user interface panel. When the load parameters dialog box opens, navigate to the working directory and select the parameter file to be loaded.



Running a Simulation

Simulation Setup

The simulation setup entries are located in the top middle region of ChipQuake™ user interface panel.



There are two basic type of simulations: "2D Simulation" and "Frequency Sweep".

The 2D simulation computes the voltage noise coupled into the analog region of the chip at a particular frequency and excitation current. This current can be estimated in multiple ways. One of the ways is described in Chapter 8 of the book "Noise Coupling in Integrated Circuits, A Practical Approach to Analysis, Modeling, and Suppression", by Dr. Cosmin Iorga. If the "3D Surface Chart" checkbox is left unchecked, the results are two-dimensional color coded voltage maps of the power supply and substrate coupling in the analog region. When "3D Surface Chart" is selected, the results are three-dimensional color coded voltage maps of the power supply and substrate coupling in the analog region.

The frequency sweep simulates the power supply and substrate noise coupled at a single location in the analog region at frequencies varying from 1Hz to 100GHz. The location is selected by the "Probe_x" and "Probe_y" numerical entries.

Starting Simulations

Click the "2D Mesh Simulation" button to start a two-dimensional simulation of the analog region. The corresponding dark blue advance bar monitors the simulation process.

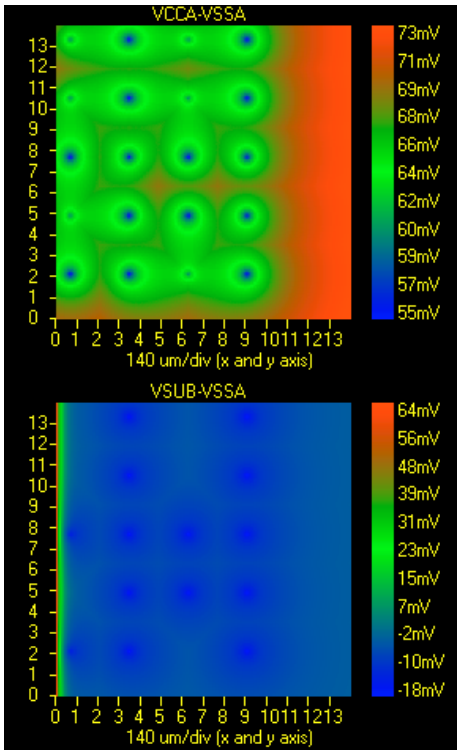
Click the "Freq. Sweep" button to start a frequency sweep simulation. The corresponding dark blue advance bar monitors the simulation process.

Important: If the ChipQuake™ window or other windows are moved or resized during the simulation, the results are not displayed. When this happens, restart the simulation by pressing the "2D Mesh Simulation" and then the "Freq. Sweep" control buttons.

Viewing the Results

2D Plots

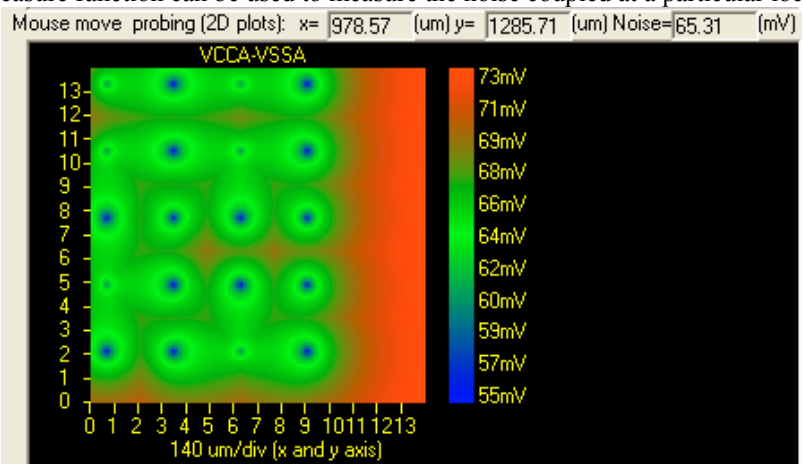
The upper graph represents the difference between the noise coupled on the positive and negative supplies in the analog region. The color coded scale is drawn in the right side of the graph. The x-y coordinates are labeled in abstract units, each unit representing a numerical physical length value displayed on the x-axis caption.



The lower graph represents the difference between the noise coupled on the substrate and negative supply in the analog region. The color coding and x-y coordinates are marked similarly as for the upper graph.

Mouse Move Probing

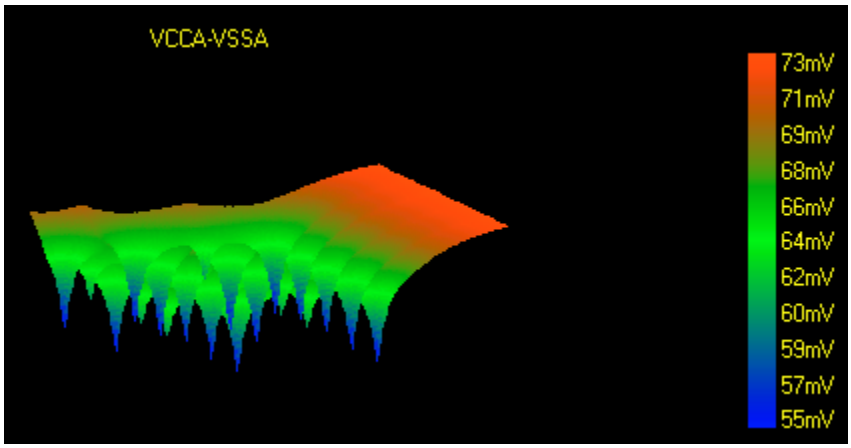
The mouse measure function can be used to measure the noise coupled at a particular location.



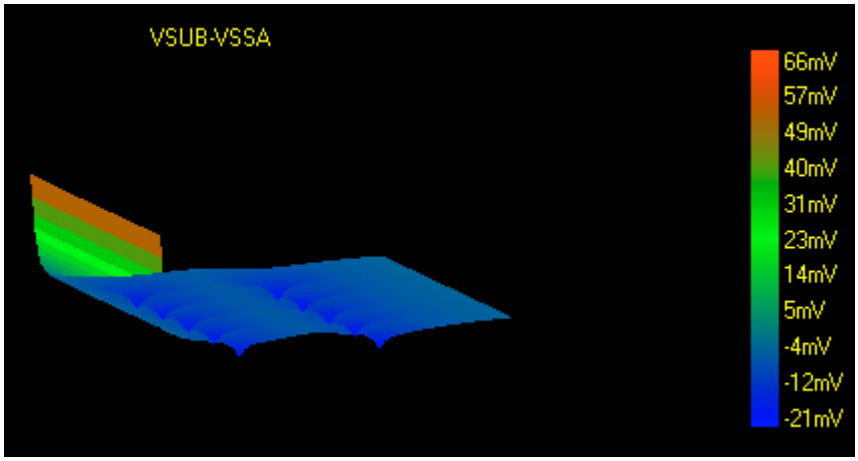
Simply move the mouse above the interested location, and the values on the top bar of the graph will display the x-y coordinates and the value of noise, as shown in the above example. The mouse move probing can be used only on the two-dimensional plots. In the three-dimensional plots the mouse move probing is also active, but the results do not have any significance.

3D Plots

The three-dimensional graphs are selected by checking the "3D Surface Chart" check box located in the simulation setup region of ChipQuake™ user interface panel. The upper plot represents the difference between the noise coupled on the positive and negative supplies in the analog region. The color coded scale is drawn in the right side of the graph.

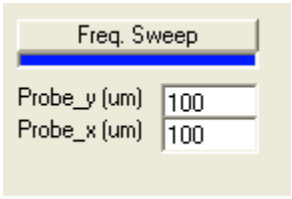


The lower plot represents the difference between the noise coupled on the substrate and the negative supply in the analog region. The color coding and x-y coordinates are marked similarly as in the upper graph.

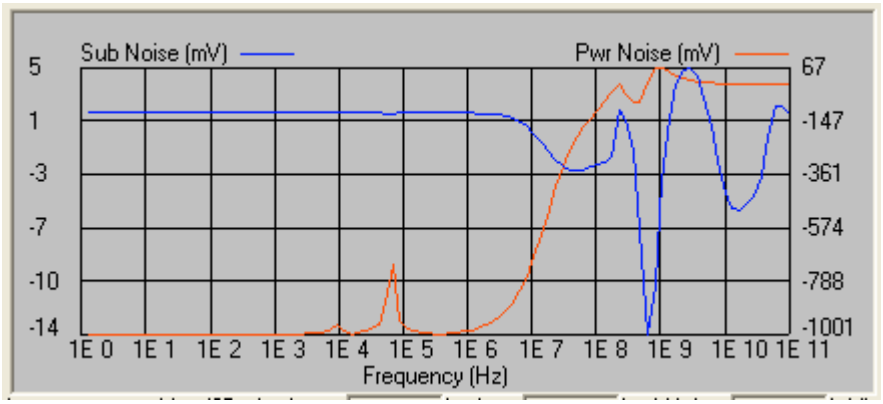


Frequency Sweep

The probing coordinates are selected through the "Probe_y" and "Probe_x" data entries. For each selection the simulation needs to be run by clicking on the "Freq. Sweep" button



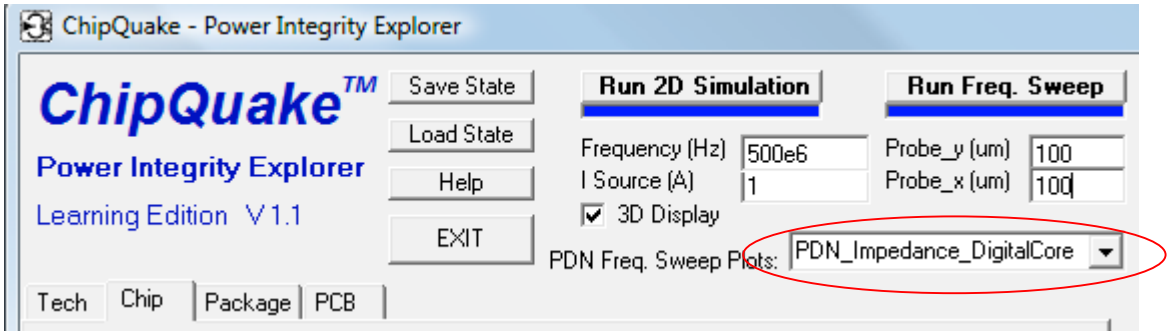
The power supply noise, labeled "Pwr Noise" in the plot, represents the difference between the noise coupled on the positive and negative supplies in the analog region. The scale is shown on the right side vertical axis.



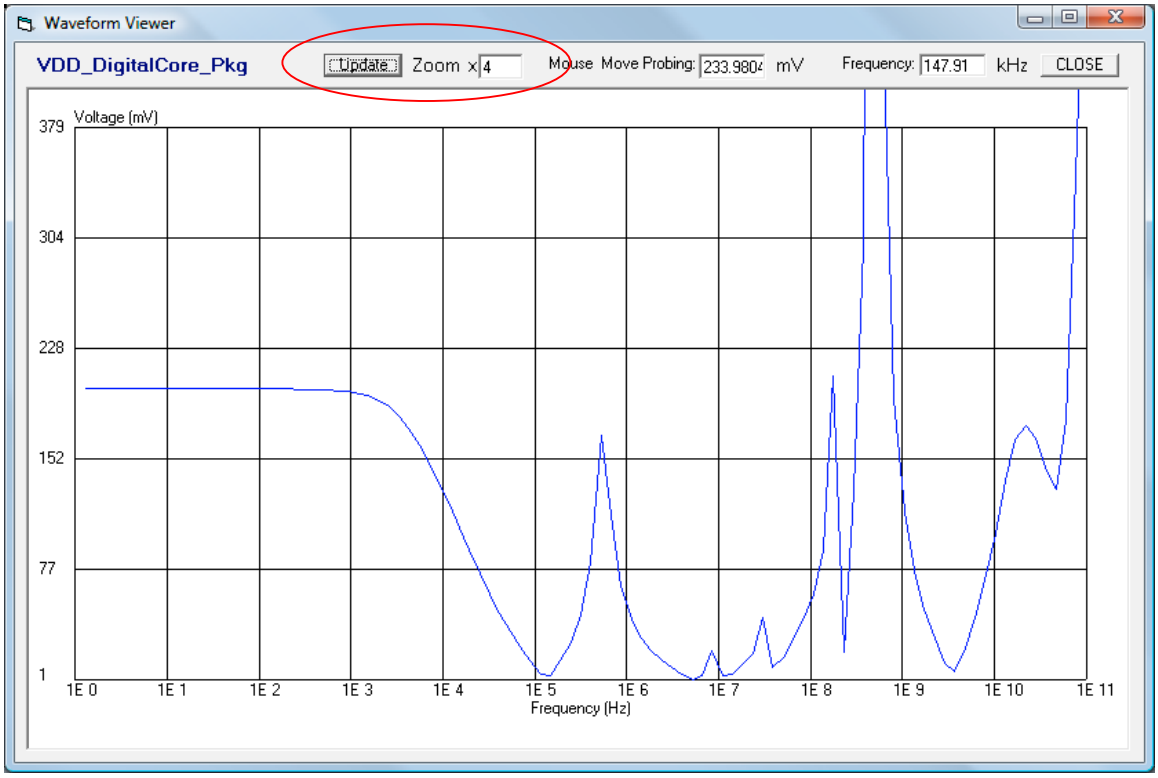
The substrate noise, labeled "Sub Noise" in the plot, represents the difference between the noise coupled on the substrate and negative supply in the analog region. The scale is shown on the left side vertical axis.

Important: If the ChipQuake™ window or other windows are moved or resized during the simulation, the results are not displayed. When this happens, restart the simulation by pressing the "2D Mesh Simulation" and then the "Freq. Sweep" control buttons.

The frequency sweep results are displayed in the waveform viewer window. Specific waveforms to be displayed are selected from the main panel using the "PDN Freq. Sweep Plots" selection box:

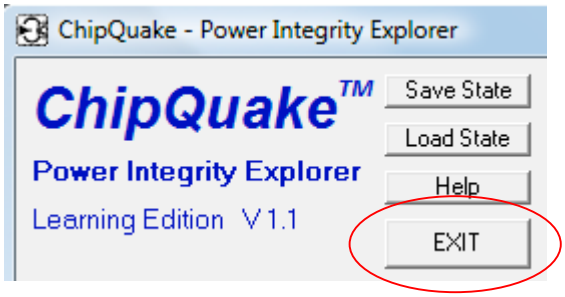


After selecting a new waveform press the "Update" button on the waveform viewer window. To zoom in to the lower amplitude values enter a zoom factor in the Zoom textbox and click "Update".



Exiting the ChipQuake Program

To exit ChipQuake™ click on the "EXIT" button located in the upper left corner region of the user interface panel.



A Note to the User

For the latest updated version of this user guide or for information on upcoming seminars and hands-on workshops on noise coupling in integrated circuits visit the NoiseCoupling.com web site: http://www.noisecoupling.com.