ChipQuakeTM Power Integrity Explorer User Guide

Learning Edition Version 1.1

NoiseCoupling.com

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ChipQuakeTM Power Integrity Explorer User Guide

Introduction

This user guide is intended to provide the user with the basic knowledge needed to setup and run **ChipQuakeTM Power Integrity Explorer** simulations.

ChipQuake[™] Power Integrity Explorer Overview

ChipQuakeTM provides fast frequency domain simulations of power integrity and noise coupling in mixed signal integrated circuits, including the effects of package and printed circuit boards (PCBs). **ChipQuakeTM** allows design engineers and system architects to visualize power integrity and noise coupling tradeoffs in a chip/package/PCB co-design.

ChipQuakeTM can be used to:

- Analyze the power integrity on the chip, package, and printed circuit board (PCB)
- Analyze the noise coupling effects on the analog regions of mixed-signal integrated circuits.
- Examine various floor-plan options, pin assignments, power grid sizes, and guard ring isolations.
- Analyze the effects of various packaging options on noise coupling.
- Explore decoupling capacitor types, values, and placement locations on the chip, package, and PCB.

INPUTS

ChipQuakeTM uses the information available in the design specifications, technology manual, package datasheet or specifications, and statistical data from typical design practices or previous designs.

OUTPUTS_

ChipQuakeTM generates two- and three-dimensional color coded maps of the substrate and power supply noise. Mouse move probing displays the noise voltage function of X-Y coordinates. ChipQuakeTM generates also frequency sweep characteristics of power supply rails on the chip, package, and PCB, and noise coupling at any X-Y coordinate in the analog region of mixed signal integrated circuits.

SIMULATION TIME

ChipQuakeTM is a fast simulator. Most simulations take less than one minute.

ACCURACY

The estimation accuracy is lower compared to that provided by post- and pre-layout extraction and simulation tools but good enough to analyze the major physical mechanisms that contribute to power integrity and noise coupling degradation in integrated circuits.

System Requirements

This section presents a set of minimum recommended system requirements for installing and running the ChipQuakeTM simulation software.

Windows XP SP2

RAM 500Mb

Hard Disk available memory 10Mb

CPU 1GHz

Display 1024 by 768

Available CDROM drive

Installation Instructions

Backup all the important data and create a system restore point in case you will want to uninstall the ChipQuakeTM software in the future.

It is recommended to exit all the running applications before starting the ChipQuakeTM installation.

Insert the ChipQuakeTM installation disk in a CDROM drive. The ChipQuakeTM installation program will run automatically. If not, open the ChipQuakeTM folder and run the Setup.exe application.

Follow the on-screen instructions to complete the installation.

If in the future you decide to uninstall the ChipQuakeTM software, you may use the "Add/Remove programs" utility available in the "Control Panel" of the Windows operating system. It is recommended to uninstall the demo version before installing to full version.

Running ChipQuake

ChipQuakeTM starts with a simulation run using default design parameters, which typically takes less than one minute. This simulation has two parts, a two-dimensional mesh simulation, and a frequency sweep. Two blue color status bars monitor both simulations. Details about setting up and running these simulations will be presented later in this user guide.

Important: If the ChipQuakeTM window or other windows are moved or resized during the simulation, the results are not displayed. When this happens, restart the simulation by pressing the "2D Mesh Simulation" and then the "Freq. Sweep" control buttons.

After the "start-up" simulations are completed, the program is ready to be used.

ChipQuake Graphical User Interface

ChipQuakeTM has a single window panel, which is used to setup, run, and view the simulation results. The following figure shows a picture of the ChipQuakeTM graphical user interface panel.



Design Input Section

The design input section is marked by label (a) in the figure above. This section contains four frames selectable through the TAB-STRIP control buttons at the top. The four sections are: Technology Data (labeled "Tech" on the Tab-Strip selection buttons), Chip Design Parameters (labeled "Chip" on the Tab-Strip selection buttons), Package Design Parameters (labeled "Package" on the Tab-Strip selection buttons), and PCB Design Parameters (labeled "PCB" on the Tab-Strip selection buttons).

Load and Save Section

The load and save section are marked by label (b). This section has a control button that allows the user to save the design input parameters into a file, and a second control button that allows the user to load the design input parameters previously stored in a file. This section contains also the control button for exiting the ChipQuakeTM program.

Simulation Setup and Run Section

The simulation setup and run section is marked by label (c). This section contains the simulation parameters and the buttons for starting simulations. There are two types of simulations: AC simulation of the entire analog region two-dimensional mesh model at a single frequency, and AC frequency sweep at a single location point in the analog region.

Results Section for Two-dimensional Mesh Simulations

The results section for distributed mesh simulation results is marked by label (d). This section displays two or three dimensional maps of the power supply and substrate noise at each location in the simulated region of the chip.

Results Section for Frequency Sweep Simulations

The results section for frequency sweep simulations is marked by label (e). This section displays the power supply and substrate noise frequency spectrum at a selectable single location in the simulated region of the chip.

An second window shows the frequency sweep results for the power distribution network as seen from the on-chip circuits, as shown in the following figure:



On the top region of this waveform viewer window there is an "Update" button, a Zoom control text box, and a mouse-move cursor that displays the frequency and amplitude value at the mouse cursor location.

The waveform viewer window can display also the frequency sweep results for the on-chip, on-package, and on-PCB analog and digital power rails. The display selection is done through a multiple-choice select box on the main ChipQuake window, as shown in the figure below:

ChipQuake - Power Integrity Explorer						
ChinQuako™	Save State	Run 2D Simulati	on Run Freq. Sweep			
ompadanc	Load State	Frequency (Hz) 500	e Probe v (um) 100			
Power Integrity Explorer	Help	I Source (A) 1	Probe_x (um) 100			
Learning Edition V1.1	EXIT	♥ 3D Display PDN Freg. Sweep Plots:	PDN_Impedance_DigitalCore			
Tech Chip Package PCB	n s_6		PDN_Impedance_DigitalCore VDD_DigitalCore_Chip VSS_DigitalCore_Chip VDD_DigitalCore_Pkg VSS_DigitalCore_Pkg			
P+ n+ n+ n C_n-diff		P+ P+	VDD_DigitalCore_PCB VSS_common_PCB VDD_Analog_Chip			

Design Data Entry

Technology Data Frame

The technology data frame can be invoked by clicking on the corresponding button in the TAB-STRIP control, located on the upper left corner of the data input section.

Tech Chip Package PCB			
VSS S G D VDD	s G	D	vss s G D
P* n* n* n* C_ndiff R_sub_cntct R_sheet_sub p-substrate	P+ C_p- R_n-well_cnl n-well C_	p+ diff cct n-well	P* n* n* C_pwel_nband mband C_nband_substate Tripple Well Option
Technology Parameters: R substrate sheet (Dhms/square) R substrate contact (Dhms/mr ² 2) R newell (Chms/mr ² 2) R vettor (Dhms/mr ² 2) R vettor an evel (Dhms/mr ² 2) C p-diffusion (PMOS S/D) ((F/um ² 2) C ndfusion (NMOS S/D) ((F/um ² 2) Triple Well Option C ndbms/ms/ms/ms/ms/ms/ms/ms/ms/ms/ms/ms/ms/m	m^2)	200 25000 25000 0.12 20000 0.25 0.25 0.25	Chip Size: Number of pirs on X-axis 20 Pirs plach (um) pin plach Y
The following parameters are es	timated fror	n previous	designs or common layout practices:
Region (Analog/Digital): Substate contact area (2) nwell contacts area (3) nwell contacts area (3) pwell area (Triple well option) (3) pwell ortacts (Triple well option) (3) nvdif S/D transistor area (3) pvdif S/D transistor area (3)	Analog 10 20 2 2 2 5 5 5	Digital 10 20 2 2 2 5 5 5	Chip Power Grid Specifications: CVDA-VSA (IF) 50 CVDA-SUSTRATE (IF) 30 CVSA-SUBSTRATE (IF) 30 Res VDA (Ohmr/square) 0.15 Res VSA (Ohmr/square) 0.15 Chip Type: Flip Chip C Wie Bond

The technology data frame consists of a symbolic drawing of a typical CMOS process, and data entry sections for technology parameters, chip type and size, and statistical parameters estimated from previous designs or common layout practices.

The symbolic drawing, shown in detail below defines graphically some of the technology parameters specific to CMOS processes.

vss s G D	VDD S G D	VSS S G D
P+ n+ n+ C_n-diff R_sub_cntct R_sheet_sub p-substrate	n+ p+ p+ C_p-diff R_n-well_cntct n-well C_n-well	p+ n+ C_p-well_n-band n-band C_n-band_substrate Tripple Well Option

These parameters are typically found under various names in the design manual of each fabrication process. The drawing has been inserted in this frame to simplify the identification of each technology parameter in the design manual.

The values of these parameters are entered in the "Technology Parameters" section, shown below.

Technology Parameters:	
R substrate sheet (Ohms/square)	200
R substrate contact (Ohms/um^2)	25000
R n-well contact (Ohms/um^2)	25000
C n-well (fF/um^2)	0.12
R vertical n-well (Ohms/um^2)	20000
C p-diffusion (PMOS S/D) (fF/um^2)	0.25
C n-diffusion (NMOS S/D) (fF/um^2)	0.25
Triple Well Option	
C n-band_sub (Triple well option) (fF/um^2)	0.12

If the chip is fabricated on a bulk substrate, the "Triple Well Option" button remains unselected. If the chip is fabricated on a substrate with isolated p-wells and n-wells, the "Triple Well Option" button needs to be selected. In this case the value of the n-band capacitance needs to be entered.

Important: The numerical values need to be entered in the same format as shown by the default parameters. If an unsupported numerical format is entered or if a spelling mistake is made, the ChipQuakeTM program runs into an error state and automatically terminates without any warning. If this happens, all the unsaved parameter values are lost. Next run of ChipQuakeTM starts with the default parameter values.

Chip Size

The width and height of the chip need to be entered as the number of pins and the spacing between the pins. The spacing between pins is also known as pin pitch. This is illustrated graphically by the two drawings representing a flip-chip and a wire-bond chip.



Statistical Parameters

The figure below shows the frame region used for entering statistical design parameters estimated from common design practices or previous projects. These statistical parameters are needed to overcome the unavailable layout information in the early stages of the design flow.

The following parameters are estimated from previous designs or common layout practices:

Region (Analog/Digital):	Analog	Digital	Chip Power Grid Specifications:
Substrate contact area (%)	10	10	C VDA-VSA (fF) 50
n-well area (%)	20	20	C VDA-SUBSTRATE (IF) 30
n-well contacts area (%)	2	2	C VSA-SUBSTRATE (fF) 30
p-well area (Triple well option) (%)	20	20	Res VDA (Ohms/square) 0.15
p-well contacts (Triple well option) (%)	2	2	Res VSA (Ohms/square) 0.15
n-diff S/D transistor area (%)	5	5	Chin Tune: 🙆 Elin Chin
p-diff S/D transistor area (%)	5	5	C Wire Bond
		-	 Wile bolid

The left side shows the entries for the estimated area percentages of substrate contacts, n-wells, n-well contacts, p-wells, p-well contacts, source and drain diffusions of NMOS transistors, and source and drain diffusions of PMOS transistors. Each statistical parameter has two entries: one for the analog region and one for the digital region. The right side shows the entries for the estimated power grid parasitic resistance and capacitance. These values can be calculated or extracted from the chip power grid or from a preliminary version, if the final version is not available in the early stages of the design.

Important: The numerical values need to be entered in the same format as shown by the default parameters. If an unsupported numerical format is entered or if a spelling mistake is made, the ChipQuakeTM program runs into an error state and automatically terminates without any warning. If this happens, all the unsaved parameter values are lost. Next run of ChipQuakeTM starts with the default parameter values.

Chip Data Input Frame

The chip data input frame can be invoked by clicking on the corresponding button in the TAB-STRIP control, located on the upper left corner of the data input section.

Tech Chip Package	PCB							
Chip Design Parar	neters —				Define t	he ana	loa rer	nion.
L pin (pH) 10	ī				I. Select	top left o	corner p	in:
B pin (Ohms) 0 0005	1			20	Top 9	-	Left	9 -
10.0003	· ' <mark>-</mark>							
Decoupling Capacitors:					2. Select	width ar	nd heigh	it (pin pitch):
CVDD-VSD (pF) 1000					Width 10		Height	10 🔻
UVDA-VSA [pF] 1000				N	umber of ¹	VDD an	d VSD p	oins:
Moat Isolation		::::::	::::: <mark>:</mark>		VDD 2	-	VSD	2 -
R_moat (Uhms) 100		::::::			1 0		1004	
Shunting Guard Ring				N	umber of '	VDA and		ins (wire bond):
R_snunt (Unms) 1					VUA 2	-	VSA	2 🗸
Digital Region	20			As	sign VDA	and V9	SA pins	(flip-chip only):
Analog Region	120						10	Analaa
	3 4		ь		8	9	10	Substrate
	V5/ •	VD4 🗸		V54 🕶			-	Touching
			-	▼ VC/		-	-	Digital
	V5/		-	V54 🗸			T	Substrate:
			-					Тор 🗌
	V 3F 🔹 🔹	VD/ •		¥3⊦ ▼				Bottom 🔲
	V9/		-					Left 🔽
8	VJA V V	-	-	• • •				Right 📃
	V9/ -				- i	- i	÷	
			- i		- i	- i	- i	
		╢──╤╟	Ţ	Ţ	Ţ	Ţ	, T	
12		┆╴╺╎	-	-			- -	
13		Î	_	_	_	_	-	
14		Î	- -	_	_	i	-	
15		i -i	-	-	-	-	-	
16		 	-	-	-	-	-	
17			-	-	-	-	-	
18			-	-	-	-	-	
19 🗸 🗸	•		-	-	-	-	-	
20			-	-	-	-	-	

The top left region contains entries for the inductance and resistance of the pins. This information is typically available in the fabrication technology design guide. The following entries are intended for the on-chip decoupling capacitance in the digital and in the analog regions. Next, there are selection buttons and parameter value entries for high resistive moat or shunting guard ring isolation techniques, if any of them are implemented on the chip.

Tech	Chip	Package	PCB]					
Chip	Chip Design Parameters Define the analog region:								
Lpin	(pH)	10		1. Select top left corner pin:					
R pin	(Ohms)	0.0005		20 Top 9 🖵 Left 9 🖵					
Deco	upling Ca	pacitors:		2. Select width and height (pin pitch):					
C VDI	D-VSD (p	F) 1000		Width 10 🗸 Height 10 🗸					
C VD/	4-VSA (pł	⁻⁾ 1000	1.5	Number of VDD and VSD pins:					
Moat	Isolation								
R_mo	at (Ohms) 100							
Shun	ting Guar	d Ring 🥅		Number of VDA and VSA pins (wire bond):					
R_sh	unt (Ohm:	s) 1		VDA 2 🗸 VSA 2 🗸					
	Digital	Region		Assign) (DA ping (film object only))					
	Analog	Region	20	Assign VDA and VSA pins (rilp-chip only):					

The top right region defines the physical placement and the size of the analog region in the overall floorplan of the chip. The physical placement is entered by the coordinates of the top-left corner measured in pin pitch units. The example shown in the figure above marks the top-left corner as the Top=6 and Left=9, which means that the analog region top left corner starts at pin 6 on the vertical axis and pin 9 on

the horizontal axis. The following "Width" and "Height" entries define the size of the analog region, also in pin pitch units. The figure in the center shows graphically the location and size of the analog region.

The following entries define the number of power supplies pins in the digital region, VDD and VSD, and in the analog region, VDA and VSA.

For wire-bond chips, the locations of the power supply pins are not specified, instead they are assumed uniformly distributed around the perimeter of the chip.

For flip-chip designs, the locations of the power supply pins are entered using the array diagram shown in the following figure.

	1	2	3	4	5	6	7	8	9	10
) 🔻	-	VS 👻	-	VD 👻	-	VS 👻	-	-	-
2	•	-	-	-	-	-	-	-	-	-
3 VC) 🔻	-	VS 👻	-	VD 👻	-	VS 👻	-	-	-
4	-	-	-	-	-	-	-	-	-	-
5 V9	-	-	VS 👻	-	VS 👻	-	VS 👻	-	-	-
6	-	-	-	-	-	-	-	-	-	-
7 VE) 🔻	-	VS 👻	-	VS 👻	-	VS 👻	-	-	-
8	-	-	-	-	-	-	-	-	-	-
9 V9	-	-	VS 👻	-	VD 👻	-	VS 👻	-	-	-
10	-	-	-	-	-	-	-	-	-	-
11	•	-	-	-	-	-	-	-	-	-
12	-	-	-	-	-	-	-	-	-	-
13	-	-	-	-	-	-	-	-	-	-
14	-	-	-	-	-	-	-	-	-	-
15	-	-	-	-	-	-	-	-	-	-
16	-	-	-	-	-	-	-	-	-	-
17	-	-	-	-	-	-	-	-	-	-
18	•	-	-	-	-	-	-	-	-	-
19	-	-	-	-	-	-	-	-	-	-
20	•	-	-	-	-	-	-	-	-	-

The pins coordinates are referenced to the analog region, and not to the overall chip. In the example above, pin (1,1) corresponds to pin (9,6) of the overall chip, where 9 is measured on the horizontal axis and 6 on the vertical axis.

To assign power or ground pins to a specific location, right-click with the mouse on the arrow select option corresponding to the chosen coordinate and select: "VDA" for positive supply, "VSA" for negative supply, or blank space for any other type of signal. Due to font size limitations, the displayed pin type shows "VD" for the "VDA", and "VS" for the "VSA".

Important: The text box entries for pin types accept typed characters besides the pre-selected "VDA", "VSA", and blank space. Do not type any characters in these text boxes. Choose only from the pre-selected options. Typing any characters may generate errors in the program execution and automatically terminate ChipQuakeTM without any warning. If this happens, all the unsaved parameter values are lost. Next run of ChipQuakeTM starts with the default parameter values.

Depending on the size and physical location, the analog region may interface with the rest of the chip on one side, two sides, three sides, or all four sides. This information is entered using the checkbox selections shown in the following figure.



Package Data Input Frame

The package data input frame can be invoked by clicking on the corresponding button in the TAB-STRIP control, located on the upper left corner of the data input section.

Tech Chip	Package P	PCB				
Package	Design Pa	rameters				
C Lead Fra	me Package	•				
Pin Inductanc	e (pH) =	20000				
Pin Resistanc	e (Ohms) =	1				
Number of pin	s on VDD =	10				
Number of pin	s on VSD =	10				
Number of pin	s on VDA =	10		C_dec		
Number of pin	s on VSA =	10		-1⊦ ←	⁴ → 💳	CUUD
🛞 BGA Pa	skage				-	
BGA pin induc	tance (pH) =	200	VDD			
BGA pin resist	ance (Ohms) =	0.3		1	L	-
Number of BG	A pins on VDD	= 10	VSD	- C1 -	C 4	
Number of BG	A pins on VSD	= 10				
Number of BG	A pins on VDA	= 10	VSA	- C3		- C6
Number of BG	A pins on VSA	= 10		1		
Dielectric Thio	hness (um)	10	VDA	T C2	- C5	
Short VSD an	d VSA on pack	age 🕅				
Package Pi	ane Lapaciti	ance				
C (- D		JUZ (VSA-VDA	J L3 (V3D-V3A	J C4 (VDD-V5)	AJ CO (VSD-VDA	AJ C6 (VDD-VDAJ
C (rir)	1	1	1	1	1	1
n (Unitis)	0.02	0.02	0.02	0.02	0.02	0.02
C (pm)	1500	1500	1500	1500	1500	1500
criable	IV ENA	IV ENA	IV ENA	I ENA	I ENA) ENA
Package D	coupling Ca	pacitors				
_	C1 (VDD-VSD) C2 (VDD-VSE)C3(VDD-VSD) C4 (VDA-VSA	A) C5 (VDA-VS4	A) C6 (VDA-VSA)
C (nF)	25	25	25	25	25	25
ESR (Ohms)	0.2	0.2	0.2	0.2	0.2	0.2
ESL (pH)	90	90	90	90	90	90
Distance (mm)	1	1	1	1	1	1
Quantity	1	1	1	1	1	1
Placed/OPEN	🔽 ENA	🔽 ENA				

If the chip is placed on a lead-frame type package, enter the pin inductance, pin resistance, and number of pins on each supply as shown in the following figure.

C Lead Frame Package	
Pin Inductance (pH) =	20000
Pin Resistance (Ohms) =	1
Number of pins on VDD =	10
Number of pins on VSD =	10
Number of pins on VDA =	10
Number of pins on VSA =	10

If the chip is placed on a BGA type package, enter the pin inductance, pin resistance, number of pins on each supply, and dielectric thickness as shown in the following figure. If a common ground plane is used for both analog and digital grounds of the chip, check the "Short VSD and VSA on package" box.

BGA Package	
BGA pin inductance (pH) =	200
BGA pin resistance (Ohms) =	0.3
Number of BGA pins on VDD =	10
Number of BGA pins on VSD =	10
Number of BGA pins on VDA =	10
Number of BGA pins on VSA =	10
Dielectric Thichness (um)	10
Short VSD and VSA on package	

Important: The numerical values need to be entered in the same format as shown by the default parameters. If an unsupported numerical format is entered or if a spelling mistake is made, the ChipQuakeTM program runs into an error state and automatically terminates without any warning. If this happens, all the unsaved parameter values are lost. Next run of ChipQuakeTM starts with the default parameter values.

For BGA packages the parasitic plane capacitance, resistance, and inductance need to be entered. The following figure illustrates graphically the definition of the plane capacitances, C1 - C6.



Depending on the physical stackup layer definition, only some of these capacitances exist. Use the checkbox labeled "Enable" as shown in the following figure to activate the corresponding capacitances. Leave unchecked the capacitances that do not exist in the stackup. Then enter the capacitance value, parasitic resistance, and parasitic inductance.

Package Plane Capacitance							
	C1 (VDD-VSD) C2 (VSA-VDA) C3 (VSD-VSA) C4 (VDD-VSA) C5 (VSD-VDA) C6 (VDD-VDA)						
C (nF)	1	1	1	1	1	1	
R (Ohms)	0.02	0.02	0.02	0.02	0.02	0.02	
L (pH)	500	500	500	500	500	500	
Enable	💌 ENA	🔽 ENA	🔽 ENA	🖂 ENA	ENA	ENA	

Some BGA packages implement decoupling capacitors. Enter the capacitor parameters as shown in the following figure. The first three columns represent decoupling capacitors on the digital power supply, and

the other three columns represent decoupling capacitors on the analog power supply. The "Distance" represents the physical separation between the capacitor and the chip, as defined in the drawing of the chip.

Package Decoupling Capacitors							
C1 (VDD-VSD) C2 (VDD-VSD) C3(VDD-VSD) C4 (VDA-VSA) C5 (VDA-VSA) C6 (VDA-VSA)							
C (nF)	25	25	25	25	25	25	
ESR (Ohms)	0.2	0.2	0.2	0.2	0.2	0.2	
ESL (pH)	90	90	90	90	90	90	
Distance (mm)	1	1	1	1	1	1	
Quantity	1	1	1	1	1	1	
Placed/OPEN	IV ENA	IV ENA	💌 ENA	💌 ENA	💌 ENA	🔽 ENA	

PCB Input Frame

The PCB data input frame can be invoked by clicking on the corresponding button in the TAB-STRIP control, located on the upper left corner of the data input section.

DECOUPLING CAPACITOR INTEGRATED CIRCUIT VDD DISTANCE (d) VS (GND) C 1 (Plane Capacitance) VDA C 2 (Plane Capacitance) C1 (VDD-VS) C2 (VDA-VS) C3 (VDD-VDA) Lplane (nH) R_pL C (nF) 1 1 R (Dhms) 0.2 0.2 0.2 LpH 500 500 500 Fnable V ENA V ENA Dielectric Thickness (um) PCB Decoupling Capacitors C1 MIDD VS1C2 MIDD VS1C3 MIDD VS1C4 MIDA VS1 C5 MIDA VS1C5 MIDA VS1 C5 MIDA	Chip Pa >BDesign	ackage PCB Paramete					
VS (GND) C 1 (Plane Capacitance) VDA C 2 (Plane Capacitance) C 3 (Plane Capacitance) PCB Plane Capacitance C 3 (Plane Capacitance) C 3 (Plane Capacitance) C (nF) 1 1 1 1 R (Dhms) 0.2 0.2 0.2 0.2 1 1 L(pH) 500 500 500 VS 1 1 PCB Decoupling Capacitors C1 M/DA/SLC2 M/DA/SLC2 M/DA/SLC3 M/DA/SLC5			DISTANC	E (d) >			
VDA C 2 (Plane Capacitance) C 3 (Plane Capacitance) PCB Plane Capacitance C1 (VDD-VS) C2 (VDA-VS) C3 (VDD-VDA) L_plane (nH) R_pl. C (nF) 1 1 1 R (Dhms) 0.2 0.2 0.2 L (pH) 500 500 VS 1 Enable V ENA V ENA ENA Dielectric Thickness (um) 10 PCB Decoupling Capacitors C1 A/DD-VC1 C2 A/DD-VC1 C2 A/DD-VS1 C2 A/DD-VS1 C5 A/DA-VS1 C5 A/	√S (GND)	- -	C 1 (Plane	Capacitance)			
PCB Plane Capacitance C1 (VDD-VS) C2 (VDA-VS) C3 (VDD-VDA) L_plane (nH) B_pl. C (nF) 1 1 1 R (Dhms) 0.2 0.2 0.2 L(pH) 500 500 VS 1 1 Enable ✓ ENA ✓ ENA ✓ ENA 10 PCB Decoupling Capacitors C1 M/DA/S1 C2 M/DA/S1 C2 M/DA/S1 C2 M/DA/S1 C3 M/DA/S1 C5 M/DA/S1	VDA	= C 2	(Plane Capacita	ance)		Plane Capacitar	nce)
PCB Plane Capacitance L_plane (nH) R_pl C1 (VDD-VS)C2 (VDA-VS) C3 (VDD-VDA) L_plane (nH) R_pl C (nF) 1 1 R (Dhms) 0.2 0.2 0.2 L (pH) 500 500 VS 1 Enable ✓ ENA ✓ ENA ✓ Dielectric Thickness (um) 10							
PCB Decoupling Capacitors	B Plane Cap C1 F) 1 Jhms) 0.2 H) 50 able ♥	acitance (VDD-VS)C2 1 2 0.2 0 500 FNA V	VDA-VS) C3 (VI 1 0.2 0 500 FNA FN	DD-VDA) VDD VDA VDA VS	L_pla 1 1 1	ane (nH) R_plan 1 1 1 1 1	e (Ohms)
PCB Decoupling Capacitors				"' Diele	ctric Thickness	(um) 10	
	3 Decoupling C1	g Capacitor: IVDD-VS1C21	S NDD-VS1C3 M	DD-VS1C4MDA-V	S1 C5 MDA-V9	SIC6 MDA-VSI	
C (nF) 1 100 10000 1 100 10000	F) 1	10	1000	0 1	100	10000	
ESR (Ohms) 0.025 0.025 0.025 0.025 0.025 0.025	3 (Ohms) 0.0	0.0	25 0.025	0.025	0.025	0.025	
ESL (pH) 30 30 30 30 30 30	. (pH) 30	30	30	30	30	30	
Distance (mm) 5 10 100 5 10 100	ance (mm) 5	10	100	5	10	100	
Quantity 1 1 1 1 1 1	antitu 🖉	1	1	1	1	1	
Placed/OPEN 🔂 ENA 🔽 ENA 🗍 ENA 🔽 ENA 🗍 ENA	anaty []						

The top drawing illustrates graphically some of the definitions and notations used in the data entry fields..



Depending on the power planes assignment in the physical stackup of the PCB, not all the plane capacitances exist. Use the checkbox labeled "Enable" as shown in the following figure to activate the corresponding capacitances. Leave unchecked the capacitances that do not exist in the stackup. Then enter the capacitance values, parasitic resistances, and parasitic inductances.

PCB Plane Capacitance							
	C1 (VDD-VS)		L_plane (nH)	R_plane (Ohm	ns)		
C (nF)	1	1	1	VDD	1	1	
R (Ohms)	0.2	0.2	0.2	VDA	1	1	
L (pH)	500	500	500	VS	1	1	
Enable	🔽 ENA	🔽 ENA	🔽 ENA	Dielectric Thic	kness (um)	10	

The data entry fields in the right side represent the inductance and resistance of the PCB power planes and the dielectric thickness.

Various decoupling capacitors are placed on the PCB in the immediate vicinity of the integrated circuit. Enter the capacitor parameters as shown in the following figure. The first three columns represent decoupling capacitors on the digital power supply, and the other three columns represent decoupling capacitors on the analog power supply. The "Distance" represents the physical separation between the capacitor and the integrated circuit, as defined in the drawing of the chip.

i ob b boodpling oupdottore							
	C1 (VDD-VS)	C2 (VDD-VS)	C3 (VDD-VS)	C4(VDA-VS)	C5 (VDA-VS)	C6 (VDA-VS)	
C (nF)	1	100	10000	1	100	10000	
ESR (Ohms)	0.025	0.025	0.025	0.025	0.025	0.025	
ESL (pH)	30	30	30	30	30	30	
Distance (mm)	5	10	100	5	10	100	
Quantity	1	1	1	1	1	1	
Placed/OPEN	ENA	🔽 ENA	ENA	ENA	🔽 ENA	ENA	

PCB Decoupling Capacitors

Important: The numerical values need to be entered in the same format as shown by the default parameters. If an unsupported numerical format is entered or if a spelling mistake is made, the ChipQuakeTM program runs into an error state and automatically terminates without any warning. If this happens, all the unsaved parameter values are lost. Next run of ChipQuakeTM starts with the default parameter values.

Save and Load Functions

Saving the Design Parameters

The design parameters can be saved at any time by clicking on the "Save State" button located in the top left region of the user interface panel. When the save parameters dialog box opens, choose a working directory and type a name for the parameter file. The file type must have text format, as shown by "param1.txt" – "param4.txt" in the example below.

Save paramete	rs				? 🛛
Save in:	🗀 chipquake		•	+ 🗈 💣 🎟	
My Recent Documents Desktop My Documents	Cd_label user_guide param1.txt param2.txt param3.txt param4.txt				
My Network Places	File name: Save as type:	Text file files(*.txt)		•	Save Cancel

Loading Previously Saved Design Parameters

Previously saved parameter files can be loaded at any time by clicking the "Load State" button located in the top left region of the user interface panel. When the load parameters dialog box opens, navigate to the working directory and select the parameter file to be loaded.

Load paramete	rs				? 🛛
Look in:	🗀 chipquake		•	+ 🗈 💣 📰 -	
My Recent Documents Desktop My Documents My Computer	Cd_label user_guide param1.txt param2.txt param3.txt param4.txt				
My Network Places	File name: Files of type:	Text file files(*.txt)		•	Open Cancel

Running a Simulation

Simulation Setup

The simulation setup entries are located in the top middle region of ChipQuakeTM user interface panel.

Run 2D Sim	ulation	Run Freq.	Sweep
Frequency (Hz) I Source (A)	500e6 1	Probe_y (um) Probe_x (um)	100 100
🔽 3D Display	·		

There are two basic type of simulations: "2D Simulation" and "Frequency Sweep".

The 2D simulation computes the voltage noise coupled into the analog region of the chip at a particular frequency and excitation current. This current can be estimated in multiple ways. One of the ways is described in Chapter 8 of the book "Noise Coupling in Integrated Circuits, A Practical Approach to Analysis, Modeling, and Suppression", by Dr. Cosmin Iorga. If the "3D Surface Chart" checkbox is left unchecked, the results are two-dimensional color coded voltage maps of the power supply and substrate coupling in the analog region. When "3D Surface Chart" is selected, the results are three-dimensional color coded voltage maps of the power supply and substrate coupling in the analog region.

The frequency sweep simulates the power supply and substrate noise coupled at a single location in the analog region at frequencies varying from 1Hz to 100GHz. The location is selected by the "Probe_x" and "Probe_y" numerical entries.

Starting Simulations

Click the "2D Mesh Simulation" button to start a two-dimensional simulation of the analog region. The corresponding dark blue advance bar monitors the simulation process.

Click the "Freq. Sweep" button to start a frequency sweep simulation. The corresponding dark blue advance bar monitors the simulation process.

Important: If the ChipQuakeTM window or other windows are moved or resized during the simulation, the results are not displayed. When this happens, restart the simulation by pressing the "2D Mesh Simulation" and then the "Freq. Sweep" control buttons.

Viewing the Results

2D Plots

The upper graph represents the difference between the noise coupled on the positive and negative supplies in the analog region. The color coded scale is drawn in the right side of the graph. The x-y coordinates are labeled in abstract units, each unit representing a numerical physical length value displayed on the x-axis caption.



The lower graph represents the difference between the noise coupled on the substrate and negative supply in the analog region. The color coding and x-y coordinates are marked similarly as for the upper graph.

Mouse Move Probing

The mouse measure function can be used to measure the noise coupled at a particular location.



Simply move the mouse above the interested location, and the values on the top bar of the graph will display the x-y coordinates and the value of noise, as shown in the above example. The mouse move probing can be used only on the two-dimensional plots. In the three-dimensional plots the mouse move probing is also active, but the results do not have any significance.

3D Plots

The three-dimensional graphs are selected by checking the "3D Surface Chart" check box located in the simulation setup region of ChipQuakeTM user interface panel. The upper plot represents the difference between the noise coupled on the positive and negative supplies in the analog region. The color coded scale is drawn in the right side of the graph.



The lower plot represents the difference between the noise coupled on the substrate and the negative supply in the analog region. The color coding and x-y coordinates are marked similarly as in the upper graph.



Frequency Sweep

The probing coordinates are selected through the "Probe_y" and "Probe_x" data entries. For each selection the simulation needs to be run by clicking on the "Freq. Sweep" button

Freq. Sweep				
Probe_y (um)	100			
Probe_x (um)	100			

The power supply noise, labeled "Pwr Noise" in the plot, represents the difference between the noise coupled on the positive and negative supplies in the analog region. The scale is shown on the right side vertical axis.



The substrate noise, labeled "Sub Noise" in the plot, represents the difference between the noise coupled on the substrate and negative supply in the analog region. The scale is shown on the left side vertical axis.

Important: If the ChipQuakeTM window or other windows are moved or resized during the simulation, the results are not displayed. When this happens, restart the simulation by pressing the "2D Mesh Simulation" and then the "Freq. Sweep" control buttons.

The frequency sweep results are displayed in the waveform viewer window. Specific waveforms to be displayed are selected from the main panel using the "PDN Freq. Sweep Plots" selection box:

ChipQuake - Power Integrity E	xplorer		
ChinQuake [™]	Save State	Run 2D Simulation	Run Freq. Sweep
Unipedanc	Load State	Frequency (Hz) 500e6	Probe_y (um) 100
Power Integrity Explorer	Help	I Source (A) 1	Probe_x (um) 100
Learning Edition V1.1	EXIT	PDN Freq Sweep Pote: PDN_Im	pedance_DigitalCore 👻
Tech Chip Package PCB		- Divined, Sweep Hous, I	

After selecting a new waveform press the "Update" button on the waveform viewer window. To zoom in to the lower amplitude values enter a zoom factor in the Zoom textbox and click "Update".

NoiseCoupling.com



Exiting the ChipQuake Program

To exit ChipQuakeTM click on the "EXIT" button located in the upper left corner region of the user interface panel.



A Note to the User

For the latest updated version of this user guide or for information on upcoming seminars and hands-on workshops on noise coupling in integrated circuits visit the NoiseCoupling.com web site: http://www.noisecoupling.com.