ABOUT THE TOOL
The Takumi Enhance-LO is unique in automatically analyzing and optimizing a layout against model-based lithography and random defect issues. It analyzes these random defects with a user-programmable critical area analysis (CAA) methodology. Using a proven two-dimensional (2D) layout modification technology and a unique quantitative cost analysis, Takumi Enhance-LO performs trade-off between various lithography and random defect issues to obtain the best optimized layout. The system’s architecture allows the addition of user-defined models for new failure mechanisms. Since the layout modification is derived from model-based analysis, it ensures protection against all yield-loss issues as modeled, whether they were encountered during process ramp-up or not. When applied to a library, the yield increases for all designs created using that library.

OVERVIEW
In the world of sub-90nm IC design, as the lithography gap widens with each new process node, it is increasingly difficult to replicate layout patterns on a wafer. Meeting minimum rule requirements does not guarantee a layout to 1) be manufacturable or 2) work as intended. In addition to the widening lithography gap, proximity effects on the layout, variations in the process and equipment-related parameters and, in general, interactions among all of these factors cause layout-related yield problems that are design and implementation specific. At these geometries, systematic and parametric defects are increasingly impacting yield in ways never seen before. Each location on a layout where such problems arise is called a hotspot. While resolution enhancement technology (RET) enables the reproduction of sub-wavelength layout on silicon, frequently the over or under correction of a layout by RET tools cause hotspots, some of which lead to silicon failure. Addressing these at the full-chip level is too late and very expensive. Being lithographic in nature, most of them occur where the layout is dense and uses minimum dimensions—typically on layers metal1 and lower at the library level. While rule-based methods address the known yield issues, model-based methods using actual foundry data offer the best protection against these yield issues mentioned above.

HANDLING MULTI-PROPERTY HOTSPOTS
Takumi Enhance-LO is architected to model all common lithographic violations seen in silicon and to detect them from looking at a layout. This includes:

- Degraded printability (poor contrast, edge placement errors—EPE’s)
- Defective contact hole or via (single contact or via, overlay margins, alignment or printing problems)
- Parametric loss due to transistor gate variations
- Random defects using CAA analysis

In addition, using a powerful Python™-based language interface, users may define custom variations to models or define a brand new custom yield-loss model and evaluate the layout against the new criteria. This allows extension of the tools to new process nodes and protects a customer’s investment in these tools.
AUTOCOST AND TRADE-OFF ANALYSIS
Not all layout defects including hotspots are fatal. Their relative impact on yield varies. Using foundry-specific data, Takumi Enhance-LO rates each hotspot in terms of its relative impact on yield—using a part per billion (ppb) score. This allows the system to trade-off between any or all yield-loss criteria to recognize and minimize the high impact hotspots and reduce the overall ppb rating for the layout.

For example, the contact cover margin is modeled for analysis and subsequent optimization by taking the various dimensions of the contact and the related polygons into account.

CO-EXIST WITH USER'S DETECTION TOOLS
If customers prefer to use hotspot data from their golden tools, they may import the OPC and litho simulation data into Takumi Enhance-LO. This includes litho contours. Using the contour data, Takumi Enhance-LO creates the cost functions corresponding to each hotspot before optimizing the layout to minimize cost.

HANDLING COMPLEX LAYOUT CONFIGURATIONS
There are two aspects of handling complex layout configurations—specification and enforcement. Takumi's Python™-based language environment for rules makes it easy to specify such complex layout requirements. For example as illustrated below, Takumi Enhance-LO may allow multiple configurations of contact cover margin on a layout. However, the configuration to be enforced depends on many factors, including the available space and the surrounding layout. Manual enforcement of such a rule is practically and economically infeasible. Such a rule can be easily specified in the Takumi environment. Takumi Enhance-LO is unique in enforcing a complex rule such as this on a layout using its 2D layout modification engine.

2D LAYOUT MODIFICATION
Takumi Enhance-LO uses a 2D automatic layout modification technology that simultaneously takes the x- and y-directional impact into account. The system is driven by cost functions and is designed to be dynamically aware of the cost and the design rules while a layout is being modified.

In addition, the system allows contact and via doubling to enhance yield. Unlike a one-dimensional system, which evaluates only the sum of the layout requirements in x and y directions for each hotspot, a 2D system evaluates the product of those layout requirements—more comprehensive analysis leading to better quality layout!

EASE OF USE
Once the system is setup with the foundry-specific information including design rules, CAA parameters, etc., using Takumi Enhance-LO to optimize a layout is very easy. The user simply specifies the class of layout hotspots needed for optimization using appropriate commands in the configuration file. For example, a user may run what-if analysis on a certain class of hotspots for individual cells using the same configuration file, but after enabling and disabling the appropriate commands inside the configuration file.

PLATFORM SUPPORT
Takumi Enhance-LO is available on a 64-bit Red Hat Linux platform.