

THIRD
EDITION

COMPUTER
SYSTEM
ARCHITECTURE

M. MORRIS MANO

This edition is manufactured in India and is authorized for sale only in India, Bangladesh, Bhutan, Pakistan, Nepal, Sri Lanka and the Maldives. Circulation of this edition outside of these territories is UNAUTHORIZED.

Contents

Preface

xv

CHAPTER ONE

Digital Logic Circuits

1

1-1	Digital Computers	1
1-2	Logic Gates	5
1-3	Boolean Algebra	7
	<i>Complement of a Function</i>	12
1-4	Map Simplification	12
	<i>Product-of-Sums Simplification</i>	16
	<i>Don't-Care Conditions</i>	18
1-5	Combinational Circuits	20
	<i>Half-Adder</i>	21
	<i>Full-Adder</i>	22
1-6	Flip-Flops	24
	<i>SR Flip-Flop</i>	24
	<i>D Flip-Flop</i>	25
	<i>JK Flip-Flop</i>	26
	<i>T Flip-Flop</i>	26
	<i>Edge-Triggered Flip-Flops</i>	27
	<i>Excitation Tables</i>	28
1-7	Sequential Circuits	29
	<i>Flip-Flop Input Equations</i>	30
	<i>State Table</i>	31
	<i>State Diagram</i>	33
	<i>Design Example</i>	33
	<i>Design Procedure</i>	36
	Problems	38
	References	40

CHAPTER TWO
Digital Components

	Digital Components	41
2-1	Integrated Circuits	41
2-2	Decoders	43
	<i>NAND Gate Decoder</i> 45	
	<i>Decoder Expansion</i> 46	
	<i>Encoders</i> 47	
2-3	Multiplexers	47
2-4	Registers	50
	<i>Register with Parallel Load</i> 50	
2-5	Shift Registers	52
	<i>Bidirectional Shift Register with Parallel Load</i> 53	
2-6	Binary Counters	55
	<i>Binary Counter with Parallel Load</i> 56	
2-7	Memory Unit	59
	<i>Random-Access Memory</i> 60	
	<i>Read-Only Memory</i> 61	
	<i>Types of ROMs</i> 62	
	Problems	63
	References	65

CHAPTER THREE
Data Representation

	Data Representation	67
3-1	Data Types	67
	<i>Number Systems</i> 68	
	<i>Octal and Hexadecimal Numbers</i> 69	
	<i>Decimal Representation</i> 72	
	<i>Alphanumeric Representation</i> 73	
3-2	Complements	74
	<i>(r - 1)'s Complement</i> 75	
	<i>(r's) Complement</i> 75	
	<i>Subtraction of Unsigned Numbers</i> 76	
3-3	Fixed-Point Representation	77
	<i>Integer Representation</i> 78	
	<i>Arithmetic Addition</i> 79	
	<i>Arithmetic Subtraction</i> 80	
	<i>Overflow</i> 80	
	<i>Decimal Fixed-Point Representation</i> 81	
3-4	Floating-Point Representation	83

3-5	Other Binary Codes	84
	<i>Gray Code</i>	85
	<i>Other Decimal Codes</i>	85
	<i>Other Alphanumeric Codes</i>	87
3-6	Error Detection Codes	87
	Problems	90
	References	91

CHAPTER FOUR

Register Transfer and Microoperations 93

4-1	Register Transfer Language	93
4-2	Register Transfer	95
4-3	Bus and Memory Transfers	97
	<i>Three-State Bus Buffers</i>	100
	<i>Memory Transfer</i>	101
4-4	Arithmetic Microoperations	102
	<i>Binary Adder</i>	103
	<i>Binary Adder-Subtractor</i>	104
	<i>Binary Incrementer</i>	105
	<i>Arithmetic Circuit</i>	106
4-5	Logic Microoperations	108
	<i>List of Logic Microoperations</i>	109
	<i>Hardware Implementation</i>	111
	<i>Some Applications</i>	111
4-6	Shift Microoperations	114
	<i>Hardware Implementation</i>	115
4-7	Arithmetic Logic Shift Unit	116
4-8	Hardware Description Languages	118
	<i>Introduction to VHDL</i>	119
	<i>Basic Framework and Syntax</i>	119
	Problems	121
	References	124

CHAPTER FIVE

Basic Computer Organization and Design 125

5-1	Instruction Codes	125
	<i>Stored Program Organization</i>	127
	<i>Indirect Address</i>	128

5-2	Computer Registers <i>Common Bus System</i>	131	129
5-3	Computer Instructions <i>Instruction Set Completeness</i>	136	134
5-4	Timing and Control		137
5-5	Instruction Cycle <i>Fetch and Decode</i>	141	141
	<i>Determine the Type of Instruction</i>	143	
	<i>Register-Reference Instructions</i>	145	
5-6	Memory-Reference Instructions		147
	<i>AND to AC</i>	147	
	<i>ADD to AC</i>	148	
	<i>LDA: Load to AC</i>	148	
	<i>STA: Store AC</i>	149	
	<i>BUN: Branch Unconditionally</i>	149	
	<i>BSA: Branch and Save Return Address</i>	149	
	<i>ISZ: Increment and Skip if Zero</i>	151	
	<i>Control Flowchart</i>	151	
5-7	Input-Output and Interrupt <i>Input-Output Configuration</i>	153	152
	<i>Input-Output Instructions</i>	154	
	<i>Program Interrupt</i>	155	
	<i>Interrupt Cycle</i>	158	
5-8	Complete Computer Description		159
5-9	Design of Basic Computer <i>Control Logic Gates</i>	160	159
	<i>Control of Registers and Memory</i>	160	
	<i>Control of Single Flip-flops</i>	164	
	<i>Control of Common Bus</i>	164	
5-10	Design of Accumulator Logic <i>Control of AC Register</i>	167	166
	<i>Adder and Logic Circuit</i>	168	
	Problems		169
	References		173

CHAPTER SIX

Programming the Basic Computer

6-1	Introduction	175
6-2	Machine Language	176

6-3	Assembly Language	181
	<i>Rules of the Language</i>	181
	<i>An Example</i>	183
	<i>Translation to Binary</i>	184
6-4	The Assembler	185
	<i>Representation of Symbolic</i>	
	<i>Program in Memory</i>	186
	<i>First Pass</i>	187
	<i>Second Pass</i>	189
6-5	Program Loops	192
6-6	Programming Arithmetic and Logic Operations	194
	<i>Multiplication Program</i>	195
	<i>Double-Precision Addition</i>	198
	<i>Logic Operations</i>	199
	<i>Shift Operations</i>	199
6-7	Subroutines	200
	<i>Subroutine Parameters and</i>	
	<i>Data Linkage</i>	202
6-8	Input-Output Programming	205
	<i>Character Manipulation</i>	206
	<i>Program Interrupt</i>	207
	Problems	210
	References	213

CHAPTER SEVEN

Microprogrammed Control 215

7-1	Control Memory	215
7-2	Address Sequencing	218
	<i>Conditional Branching</i>	219
	<i>Mapping of Instruction</i>	221
	<i>Subroutines</i>	222
7-3	Microprogram Example	222
	<i>Computer Configuration</i>	222
	<i>Microinstruction Format</i>	224
	<i>Symbolic Microinstructions</i>	227
	<i>The Fetch Routine</i>	228
	<i>Symbolic Microprogram</i>	229
	<i>Binary Microprogram</i>	231

7-4	Design of Control Unit		
	<i>Microprogram Sequencer</i>	234	233
	Problems		237
	References		240

CHAPTER EIGHT

Central Processing Unit

			243
8-1	Introduction		243
8-2	General Register Organization		243
	<i>Control Word</i>	245	244
	<i>Examples of Microoperations</i>	248	
8-3	Stack Organization		249
	<i>Register Stack</i>	249	
	<i>Memory Stack</i>	251	
	<i>Reverse Polish Notation</i>	253	
	<i>Evaluation of Arithmetic Expressions</i>	255	
8-4	Instruction Formats		257
	<i>Three-Address Instructions</i>	260	
	<i>Two-Address Instructions</i>	260	
	<i>One-Address Instructions</i>	261	
	<i>Zero-Address Instructions</i>	261	
	<i>RISC Instructions</i>	261	
8-5	Addressing Modes		262
	<i>Numerical Example</i>	266	
8-6	Data Transfer and Manipulation		268
	<i>Data Transfer Instructions</i>	269	
	<i>Data Manipulation Instructions</i>	270	
	<i>Arithmetic Instructions</i>	271	
	<i>Logical and Bit Manipulation Instructions</i>	272	
	<i>Shift Instructions</i>	273	
8-7	Program Control		275
	<i>Status Bit Conditions</i>	276	
	<i>Conditional Branch Instructions</i>	277	
	<i>Subroutine Call and Return</i>	280	
	<i>Program Interrupt</i>	281	
	<i>Types of Interrupts</i>	283	
8-8	Reduced Instruction Set Computer (RISC)		284
	<i>CISC Characteristics</i>	285	
	<i>RISC Characteristics</i>	286	

<i>Overlapped Register Windows</i>	287	
<i>Berkeley RISC I</i>	290	
Problems		293
References		299

CHAPTER NINE

Pipeline and Vector Processing 301

9-1	Parallel Processing		301
9-2	Pipelining		304
	<i>General Considerations</i>	306	
9-3	Arithmetic Pipeline		309
9-4	Instruction Pipeline		312
	<i>Example: Four-Segment Instruction Pipeline</i>		313
	<i>Data Dependency</i>	315	
	<i>Handling of Branch Instructions</i>	316	
9-5	RISC Pipeline		317
	<i>Example: Three-Segment Instruction Pipeline</i>		318
	<i>Delayed Load</i>	319	
	<i>Delayed Branch</i>	320	
9-6	Vector Processing		321
	<i>Vector Operations</i>	323	
	<i>Matrix Multiplication</i>	324	
	<i>Memory Interleaving</i>	326	
	<i>Superscalar Processors</i>	327	
	<i>Supercomputers</i>	328	
9-7	Array Processors		329
	<i>Attached Array Processor</i>	329	
	<i>SIMD Array Processor</i>	330	
	Problems		331
	References		333

CHAPTER TEN

Computer Arithmetic 335

10-1	Introduction		335
10-2	Addition and Subtraction		336
	<i>Addition and Subtraction with Signed-Magnitude Data</i>	337	

	<i>Hardware Implementation</i>	338	
	<i>Hardware Algorithm</i>	339	
	<i>Addition and Subtraction with Signed-2's Complement Data</i>	340	
10-3	<i>Multiplication Algorithms</i>		342
	<i>Hardware Implementation for Signed-Magnitude Data</i>	343	
	<i>Hardware Algorithm</i>	344	
	<i>Booth Multiplication Algorithm</i>	345	
	<i>Array Multiplier</i>	348	
10-4	<i>Division Algorithms</i>		350
	<i>Hardware Implementation for Signed-Magnitude Data</i>	351	
	<i>Divide Overflow</i>	353	
	<i>Hardware Algorithm</i>	354	
	<i>Other Algorithms</i>	355	
10-5	<i>Floating-Point Arithmetic Operations</i>		356
	<i>Basic Considerations</i>	356	
	<i>Register Configuration</i>	359	
	<i>Addition and Subtraction</i>	360	
	<i>Multiplication</i>	362	
	<i>Division</i>	364	
10-6	<i>Decimal Arithmetic Unit</i>		365
	<i>BCD Adder</i>	367	
	<i>BCD Subtraction</i>	370	
10-7	<i>Decimal Arithmetic Operations</i>		371
	<i>Addition and Subtraction</i>	373	
	<i>Multiplication</i>	373	
	<i>Division</i>	376	
	<i>Floating-Point Operations</i>	378	
	<i>Problems</i>		378
	<i>References</i>		382

CHAPTER ELEVEN

	Input-Output Organization		383
11-1	<i>Peripheral Devices</i>		383
	<i>ASCII Alphanumeric Characters</i>	385	
11-2	<i>Input-Output Interface</i>		387
	<i>I/O Bus and Interface Modules</i>	388	
	<i>I/O versus Memory Bus</i>	389	

	<i>Isolated versus Memory-Mapped I/O</i>	390	
	<i>Example of I/O Interface</i>	391	
11-3	<i>Asynchronous Data Transfer</i>		393
	<i>Strobe Control</i>	394	
	<i>Handshaking</i>	395	
	<i>Asynchronous Serial Transfer</i>	398	
	<i>Asynchronous Communication Interface</i>		400
	<i>First-In, First-Out Buffer</i>	402	
11-4	<i>Modes of Transfer</i>		404
	<i>Example of Programmed I/O</i>	405	
	<i>Interrupt-Initiated I/O</i>	408	
	<i>Software Considerations</i>	408	
11-5	<i>Priority Interrupt</i>		409
	<i>Daisy-Chaining Priority</i>	410	
	<i>Parallel Priority Interrupt</i>	411	
	<i>Priority Encoder</i>	413	
	<i>Interrupt Cycle</i>	414	
	<i>Software Routines</i>	415	
	<i>Initial and Final Operations</i>	416	
11-6	<i>Direct Memory Access (DMA)</i>		417
	<i>DMA Controller</i>	418	
	<i>DMA Transfer</i>	420	
11-7	<i>Input-Output Processor (IOP)</i>		422
	<i>CPU-IOP Communication</i>	424	
	<i>IBM 370 I/O Channel</i>	425	
	<i>Intel 8089 IOP</i>	429	
11-8	<i>Serial Communication</i>		431
	<i>Character-Oriented Protocol</i>	434	
	<i>Transmission Example</i>	435	
	<i>Data Transparency</i>	438	
	<i>Bit-Oriented Protocol</i>	439	
	<i>Problems</i>		441
	<i>References</i>		444

CHAPTER TWELVE

	Memory Organization		447
12-1	<i>Memory Hierarchy</i>		447
12-2	<i>Main Memory</i>		450
	<i>RAM and ROM Chips</i>	451	

	<i>Memory Address Map</i>	452	
	<i>Memory Connection to CPU</i>	454	
12-3	Auxiliary Memory		454
	<i>Magnetic Disks</i>	456	
	<i>Magnetic Tape</i>	457	
12-4	Associative Memory		458
	<i>Hardware Organization</i>	459	
	<i>Match Logic</i>	461	
	<i>Read Operation</i>	462	
	<i>Write Operation</i>	463	
12-5	Cache Memory		464
	<i>Associative Mapping</i>	466	
	<i>Direct Mapping</i>	467	
	<i>Set-Associative Mapping</i>	469	
	<i>Writing into Cache</i>	470	
	<i>Cache Initialization</i>	471	
12-6	Virtual Memory		471
	<i>Address Space and Memory Space</i>	472	
	<i>Address Mapping Using Pages</i>	474	
	<i>Associative Memory Page Table</i>	476	
	<i>Page Replacement</i>	477	
12-7	Memory Management Hardware		478
	<i>Segmented-Page Mapping</i>	479	
	<i>Numerical Example</i>	481	
	<i>Memory Protection</i>	484	
	Problems		485
	References		488

CHAPTER THIRTEEN

Multiprocessors 491

13-1	Characteristics of Multiprocessors		491
13-2	Interconnection Structures		493
	<i>Time-Shared Common Bus</i>	493	
	<i>Multipoint Memory</i>	495	
	<i>Crossbar Switch</i>	496	
	<i>Multistage Switching Network</i>	498	
	<i>Hypercube Interconnection</i>	500	
13-3	Interprocessor Arbitration		502
	<i>System Bus</i>	502	

	<i>Serial Arbitration Procedure</i>	504	
	<i>Parallel Arbitration Logic</i>	505	
	<i>Dynamic Arbitration Algorithms</i>	507	
13-4	Interprocessor Communication and Synchronization		507
	<i>Interprocessor Synchronization</i>	509	
	<i>Mutual Exclusion with a Semaphore</i>	509	
	Problems		511
	References		512

	Index	513
--	--------------	-----