


Also available as  Book

 SPECIAL
INDIAN
EDITION

DIGITAL PRINCIPLES AND APPLICATIONS

Donald P Leach | Albert Paul Malvino | Goutam Saha

8e



**Mc
Graw
Hill
Education**

Contents

Preface to the Eighth Edition (SIE)

Preface to the Fifth Edition

1. Digital Principles

- 1.1 Definitions for Digital Signals 2
- 1.2 Digital Waveforms 4
- 1.3 Digital Logic 8
- 1.4 Moving and Storing Digital Information 14
- 1.5 Digital Operations 18
- 1.6 Digital Computers 23
- 1.7 Digital Integrated Circuits 27
- 1.8 Digital IC Signal Levels 33
 - Summary* 36
 - Glossary* 36
 - Problems* 37

2. Digital Logic

- 2.1 The Basic Gates—NOT, OR, AND 41
- 2.2 Universal Logic Gates—NOR, NAND 49
- 2.3 AND-OR-Invert Gates 58
- 2.4 Positive and Negative Logic 60
- 2.5 Introduction to HDL 62
 - Summary* 69
 - Glossary* 70
 - Problems* 70
 - Laboratory Experiment* 74

3. Combinational Logic Circuits

- 3.1 Boolean Laws and Theorems 76
- 3.2 Sum-of-Products Method 84
- 3.3 Truth Table to Karnaugh Map 87
- 3.4 Pairs, Quads, and Octets 89
- 3.5 Karnaugh Simplifications 92
- 3.6 Don't-care Conditions 96
- 3.7 Product-of-sums Method 98
- 3.8 Product-of-sums Simplification 101
- 3.9 Five Variable Karnaugh Map 105
- 3.10 Minimization of Multiple-Output Function Using Karnaugh Map 107
- 3.11 Simplification by Quine-McClusky Method 110

xi

xv

1

41

75

- 3.12 Hazards and Hazard Covers 114
- 3.11 HDL Implementation Models 118
 - Problem Solving with Multiple Methods* 120
 - Summary* 121
 - Glossary* 122
 - Problems* 122
 - Laboratory Experiment* 126

4. Data-Processing Circuits

129

- 4.1 Multiplexers 129
- 4.2 Demultiplexers 138
- 4.3 1-of-16 Decoder 141
- 4.4 BCD-to-decimal Decoders 144
- 4.5 Seven-segment Decoders 147
- 4.6 Encoders 149
- 4.7 Exclusive-OR Gates 152
- 4.8 Parity Generators and Checkers 154
- 4.9 Magnitude Comparator 157
- 4.10 Read-only Memory 159
- 4.11 Programmable Array Logic 165
- 4.12 Programmable Logic Arrays 167
- 4.13 Troubleshooting with a Logic Probe 169
- 4.14 HDL Implementation of Data Processing Circuits 170
 - Problem Solving with Multiple Methods* 172
 - Summary* 174
 - Glossary* 174
 - Problems* 175
 - Laboratory Experiment* 180

5. Number Systems and Codes

182

- 5.1 Binary Number System 182
- 5.2 Radix Representation of Numbers 184
- 5.3 Binary-to-decimal Conversion 185
- 5.4 Fixed Point Representation 188
- 5.5 Decimal-to-binary Conversion 189
- 5.6 Octal Numbers 192
- 5.7 Hexadecimal Numbers 196
- 5.8 The ASCII Code 203
- 5.9 The Excess-3 Code 205
- 5.10 The Gray Code 206
- 5.11 Troubleshooting with a Logic Pulser 207
- 5.12 Error Detection and Correction 209
 - Problem Solving with Multiple Methods* 211
 - Summary* 212
 - Glossary* 213
 - Problems* 213
 - Laboratory Experiment* 218

6. Arithmetic Circuits

- 6.1 Binary Addition 220
- 6.2 Binary Subtraction 224
- 6.3 Unsigned Binary Numbers 225
- 6.4 Sign-magnitude Numbers 227
- 6.5 2's Complement Representation 229
- 6.6 2's Complement Arithmetic 233
- 6.7 Arithmetic Building Blocks 239
- 6.8 The Adder-subtractor 241
- 6.9 Fast Adder 245
- 6.10 Arithmetic Logic Unit 248
- 6.11 Binary Multiplication and Division 250
- 6.12 Arithmetic Circuits Using HDL 250
 - Problem Solving with Multiple Methods* 252
 - Summary* 253
 - Glossary* 254
 - Problems* 254
 - Laboratory Experiment* 256

7. Clocks and Timing Circuits

- 7.1 Clock Waveforms 257
- 7.2 TTL Clock 262
- 7.3 Schmitt Trigger 263
- 7.4 555 Timer—Astable 266
- 7.5 555 Timer—Monostable 269
- 7.6 Monostables with Input Logic 271
- 7.7 Pulse-forming Circuits 275
 - Problem Solving with Multiple Methods* 277
 - Summary* 278
 - Glossary* 279
 - Problems* 279
 - Laboratory Experiment* 281

8. Flip-Flops

- 8.1 RS FLIP-FLOPs 284
- 8.2 Gated FLIP-FLOPs 289
- 8.3 Edge-triggered RS FLIP-FLOPs 292
- 8.4 Edge-triggered D FLIP-FLOPs 294
- 8.5 Edge-triggered JK FLIP-FLOPs 296
- 8.6 FLIP-FLOP Timing 298
- 8.7 Edge Triggering through Input Lock Out 299
- 8.8 JK Master-slave FLIP-FLOPs 301
- 8.9 Switch Contact Bounce Circuits 302
- 8.10 Various Representations of FLIP-FLOPs 303
- 8.11 Analysis of Sequential Circuits 306
- 8.12 Conversion of FLIP-FLOPs: A Synthesis Example 309
- 8.13 HDL Implementation of FLIP-FLOP 311

257

283

	<i>Problem Solving with Multiple Methods</i>	314	
	<i>Summary</i>	316	
	<i>Glossary</i>	316	
	<i>Problems</i>	317	
	<i>Laboratory Experiment</i>	319	
9. Registers			
9.1	Types of Registers	322	
9.2	Serial In–Serial Out	323	
9.3	Serial In–Parallel Out	326	
9.4	Parallel In–Serial Out	329	
9.5	Parallel In–Parallel Out	333	
9.6	Universal Shift Register	337	
9.7	Applications of Shift Registers	338	
9.8	Register Implementation in HDL	349	
	<i>Problem Solving with Multiple Methods</i>	350	
	<i>Summary</i>	351	
	<i>Glossary</i>	352	
	<i>Problems</i>	352	
	<i>Laboratory Experiment</i>	356	
10. Counters			
10.1	Asynchronous Counters	358	
10.2	Decoding Gates	362	
10.3	Synchronous Counters	365	
10.4	Changing the Counter Modulus	373	
10.5	Decade Counters	379	
10.6	Presetable Counters	384	
10.7	Counter Design as a Synthesis Problem	392	
10.8	A Digital Clock	397	
10.9	Counter Design using HDL	400	
	<i>Problem Solving with Multiple Methods</i>	402	
	<i>Summary</i>	403	
	<i>Glossary</i>	404	
	<i>Problems</i>	404	
	<i>Laboratory Experiment</i>	406	
11. Design of Synchronous and Asynchronous Sequential Circuits			
PART A: Design of Synchronous Sequential Circuit	409		408
11.1	Model Selection	409	
11.2	State Transition Diagram	410	
11.3	State Synthesis Table	412	
11.4	Design Equations and Circuit Diagram	414	
11.5	Implementation using Read Only Memory	416	
11.6	Algorithmic State Machine	420	
11.7	State Reduction Technique	425	



PART B: Asynchronous Sequential Circuit	429	
11.8 Analysis of Asynchronous Sequential Circuit	430	
11.9 Problems with Asynchronous Sequential Circuits	433	
11.10 Design of Asynchronous Sequential Circuit	435	
11.11 FSM Implementation in HDL	439	
<i>Problem Solving with Multiple Methods</i>	441	
<i>Summary</i>	448	
<i>Glossary</i>	448	
<i>Problems</i>	449	
<i>Laboratory Experiment</i>	451	
12. D/A Conversion and A/D Conversion		454
12.1 Variable, Resistor Networks	455	
12.2 Binary Ladders	458	
12.3 D/A Converters	463	
12.4 D/A Accuracy and Resolution	470	
12.5 A/D Converter—Simultaneous Conversion	471	
12.6 A/D Converter—Counter Method	474	
12.7 Continuous A/D Conversion	477	
12.8 A/D Techniques	480	
12.9 Dual-slope A/D Conversion	483	
12.10 A/D Accuracy and Resolution	487	
<i>Summary</i>	488	
<i>Glossary</i>	489	
<i>Problems</i>	489	
13. Memory		492
13.1 Basic Terms and Ideas	493	
13.2 Memory Read and Write	495	
13.3 Memory Addressing	499	
13.4 ROMs, PROMs, and EPROMs	504	
13.5 RAMs	509	
13.6 Sequential Programmable Logic Devices	516	
13.7 Content Addressable Memory	519	
13.8 Magnetic Memory	520	
<i>Summary</i>	528	
<i>Glossary</i>	528	
<i>Problems</i>	529	
14. Digital Integrated Circuits		532
14.1 Switching Circuits	533	
14.2 7400 TTL	538	
14.3 Voltage Transfer Characteristics	541	
14.4 TTL Parameters	543	
14.5 TTL Overview	550	



14.6 Open-collector Gates 552

14.7 Three-state TTL Devices 554

14.8 External Drive for TTL Loads 556

14.9 TTL Driving External Loads 559

14.10 74C00 CMOS 560

14.11 CMOS Characteristics 563

14.12 TTL-to-CMOS Interface 567

14.13 CMOS-to-TTL Interface 569

14.14 Current Tracers 571

Summary 573

Glossary 574

Problems 575

15. Applications 581

15.1 Multiplexing Displays 582

15.2 Frequency Counters 588

15.3 Time Measurement 593

15.4 Using the ADC0804 594

15.5 Microprocessor-compatible A/D Converters 600

15.6 Digital Voltmeters 608

Summary 614

Problems 614

16. A Simple Computer Design 616

16.1 Building Blocks 617

16.2 Register Transfer Language 620

16.3 Execution of Instructions, Macro and Micro Operations 622

16.4 Design of Control Unit 625

16.5 Programming Computer 628

Summary 635

Glossary 635

Problems 636

Appendix 1: Binary-Hexadecimal-Decimal Equivalents 638

Appendix 2: 2's Complement Representation 644

Appendix 3: TTL Devices 648

Appendix 4: CMOS Devices 651

Appendix 5: Codes 653

Appendix 6: BCD Codes 656

Appendix 7: Overview of IEEE Std. 91-1984, Explanation of Logic Symbols 661

Appendix 8: Pinout Diagrams 666

Appendix 9: Answers to Selected Odd-Numbered Problems 670

Index